

**Power Block Diagram**  
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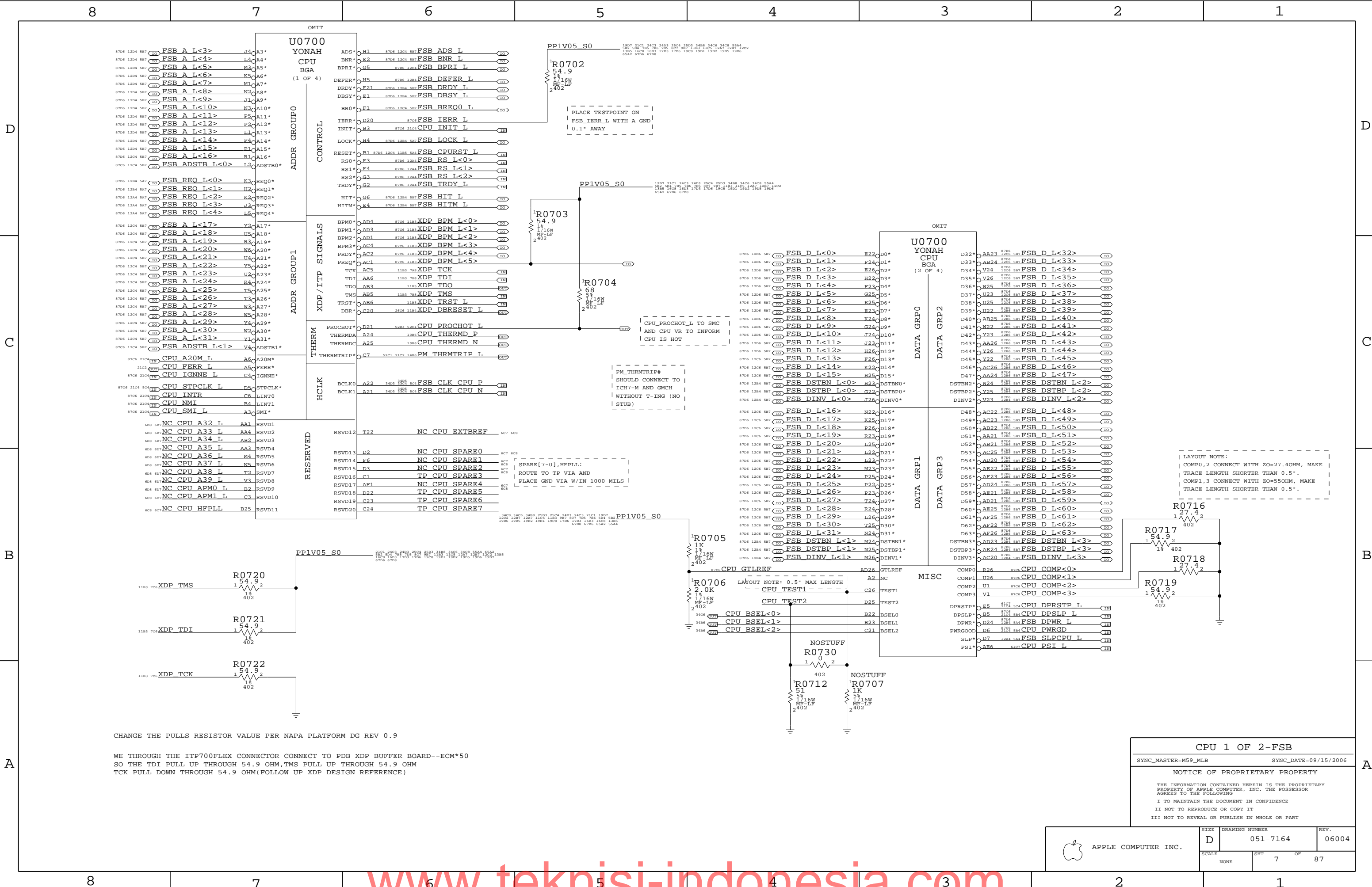
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	SCALE NONE	SHT 3	OF 87

[illegible]

	8	7	6	5	4	3	2	1		
	Power Supply NO_TESTS				Functional Test Points					
	NO_TEST EXPOSED_VIA									
	TRUE IMVP6 RBIAS 61C7									
	TRUE P5VS5 RUNSS 62C5 66A6									
	TRUE P1V5S0 RUNSS 62C4 66C6									
	TRUE P2V5S3 MODE									
	TRUE P2V5S3_SHDNRT									
	TRUE P1V2S3 RT 63B6									
	TRUE P1V2S3 RUNSS 41C4 63B7									
	TRUE P1V8S3_COMP									
	TRUE P1V8S3_FSET									
	TRUE P3V3S5_COMP 65C6									
	TRUE P3V3S5_FSET 65D6									
	TRUE P1V05S0_COMP 65A7									
	TRUE P1V05S0_FSET 65B7									
	TRUE P3V42Q3H_FB 66C3									
	TRUE GPUVCORE_COMP 71C7									
	TRUE GPUVCORE_FSET 71C7									
	TRUE GPUBBP_ADJ 71B7									







CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM\*50  
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM  
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

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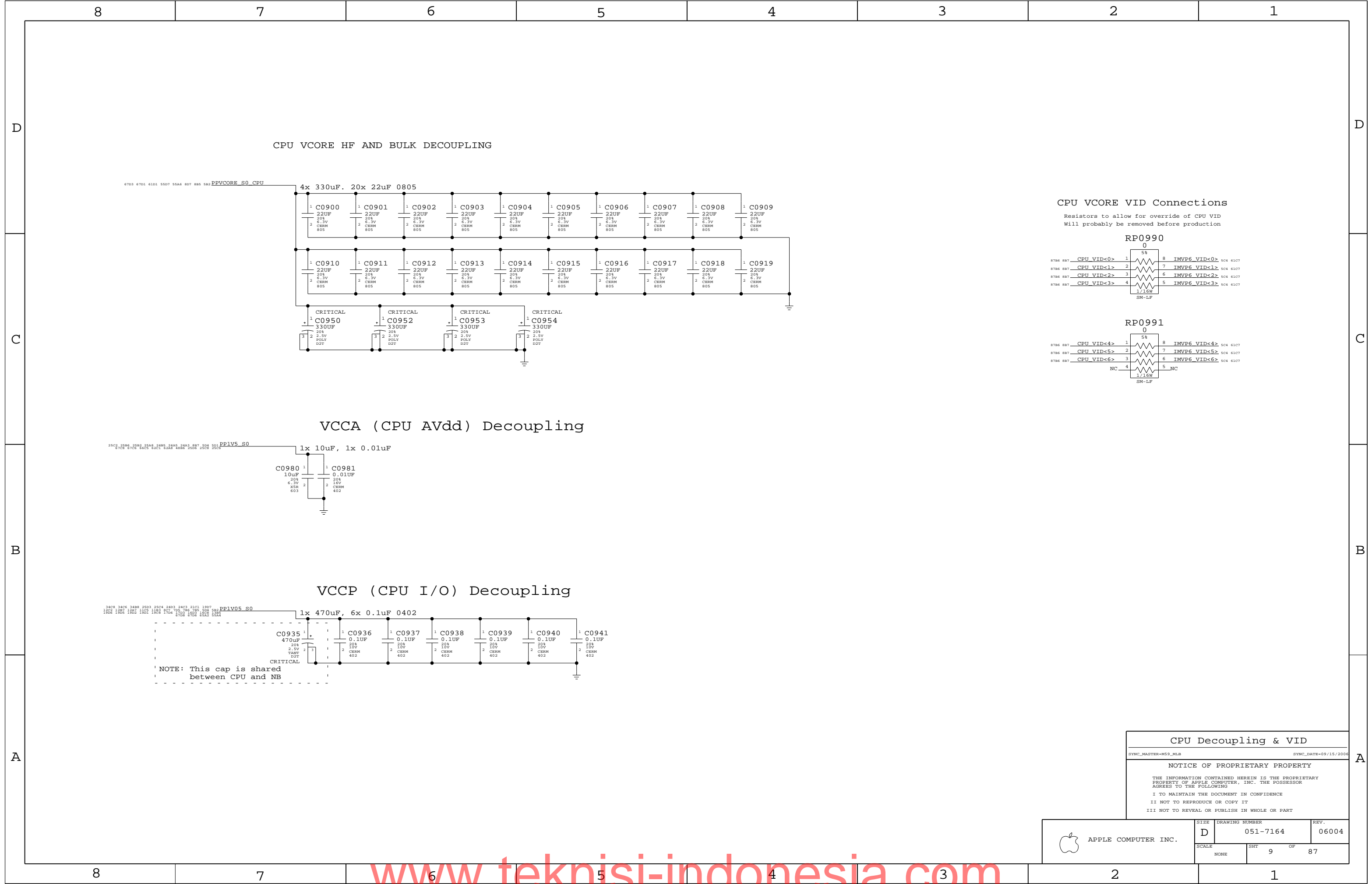
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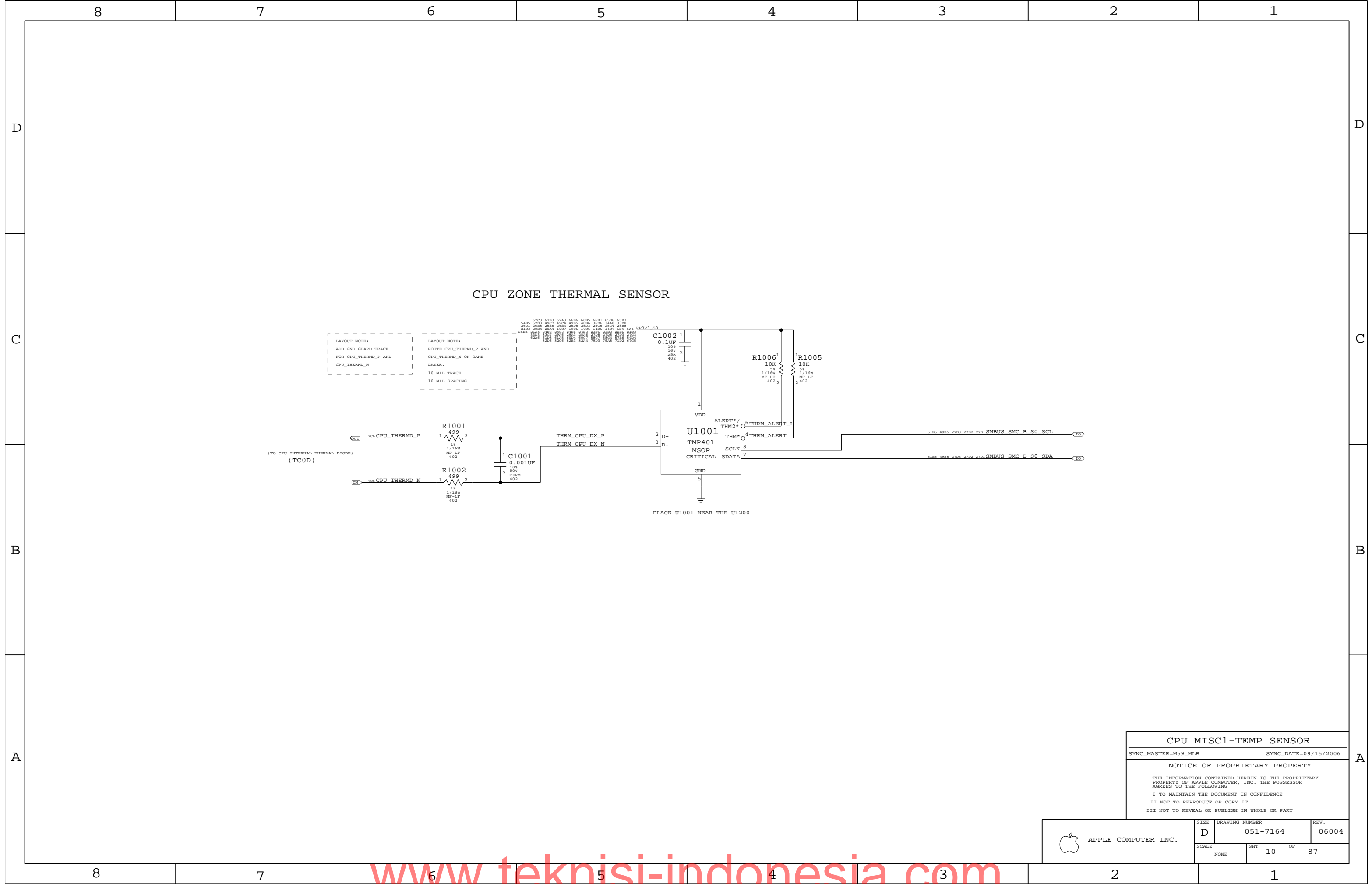
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CPU MISC1-TEMP SENSOR

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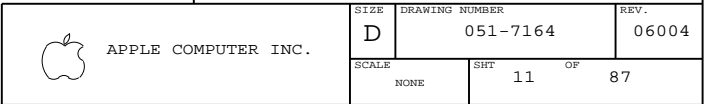
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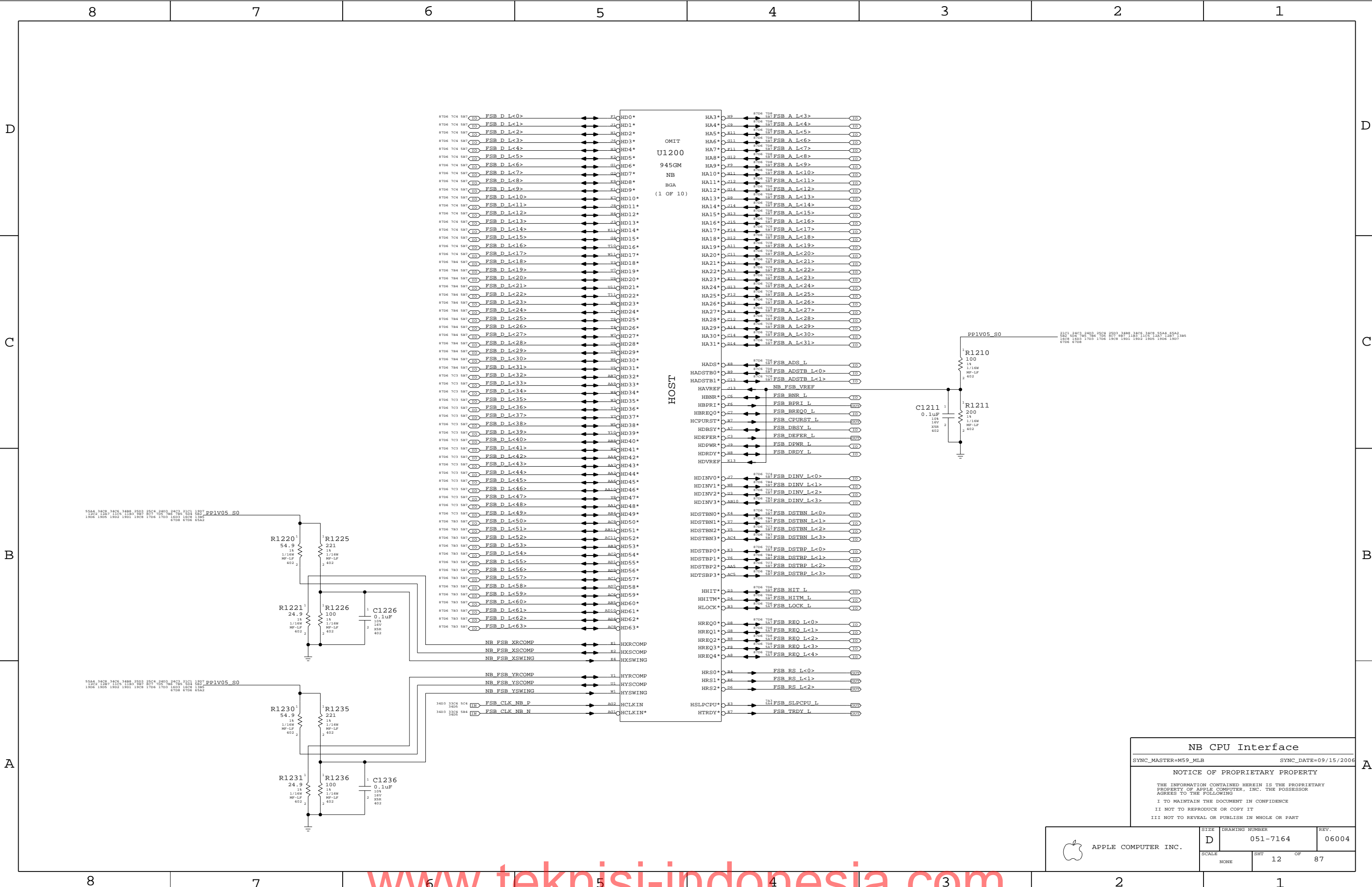
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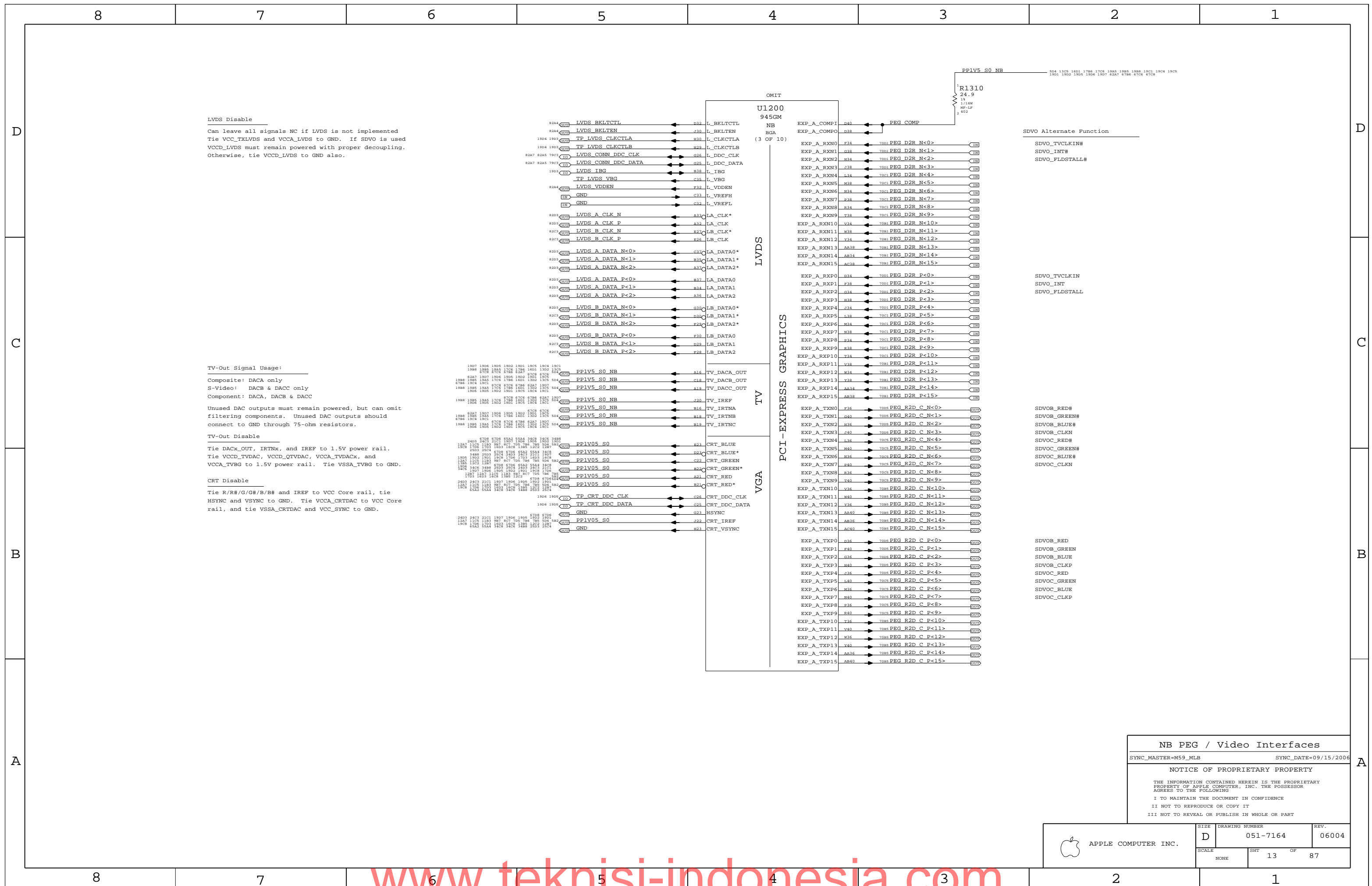
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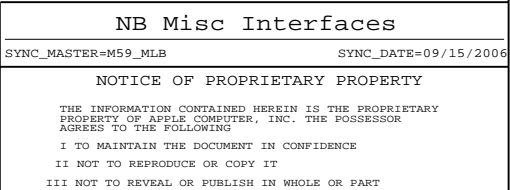
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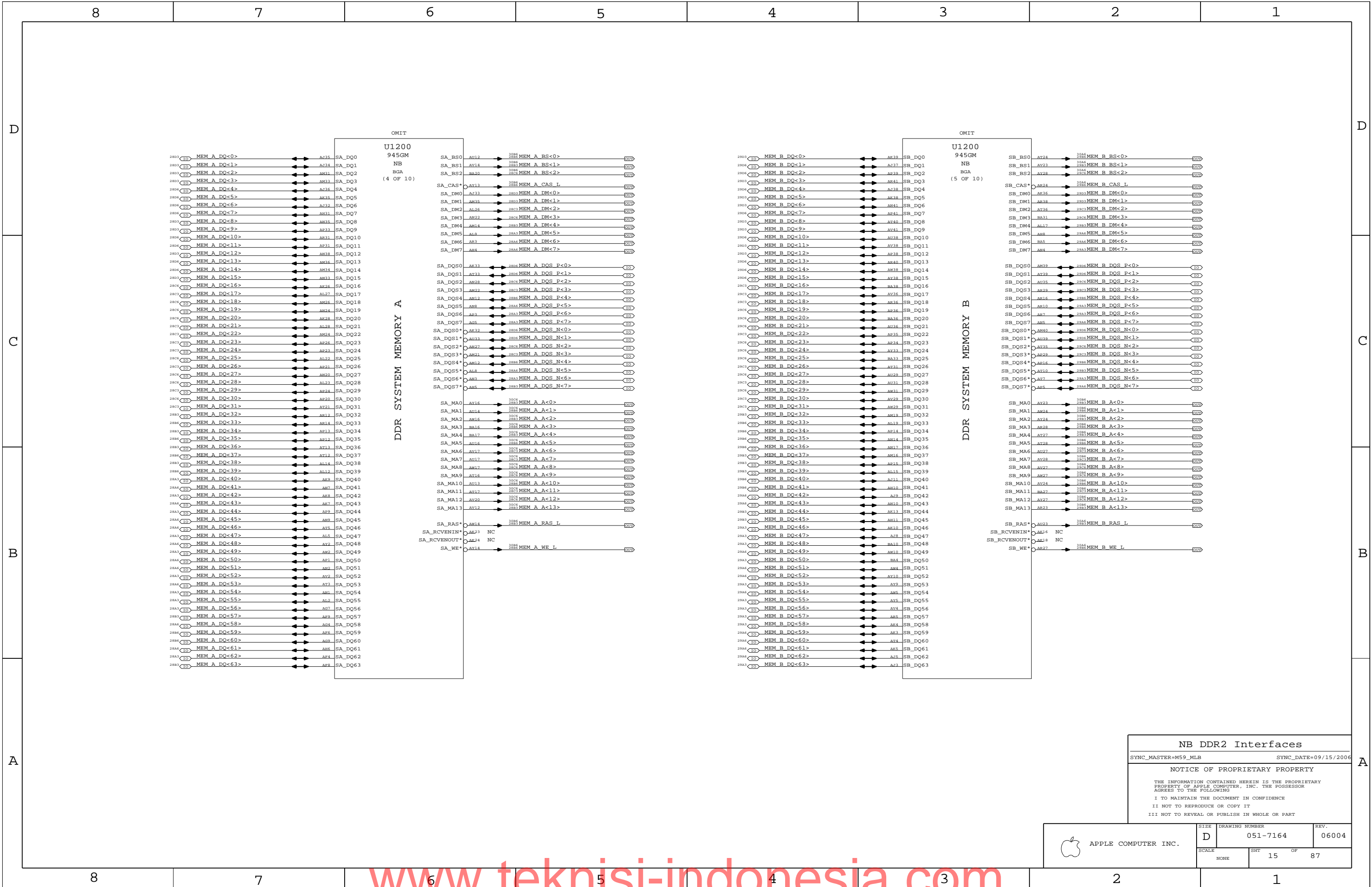












NB DDR2 Interfaces

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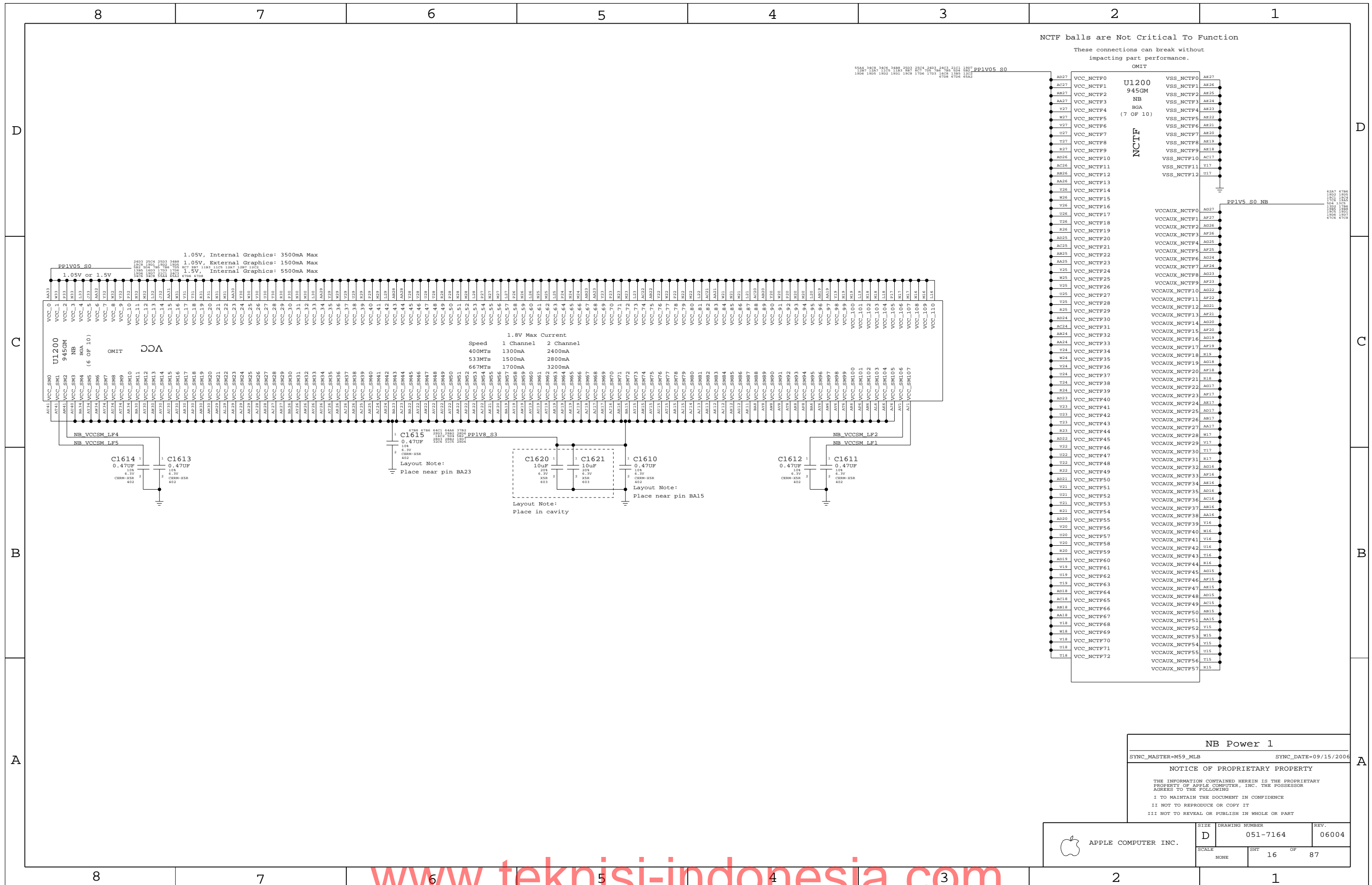
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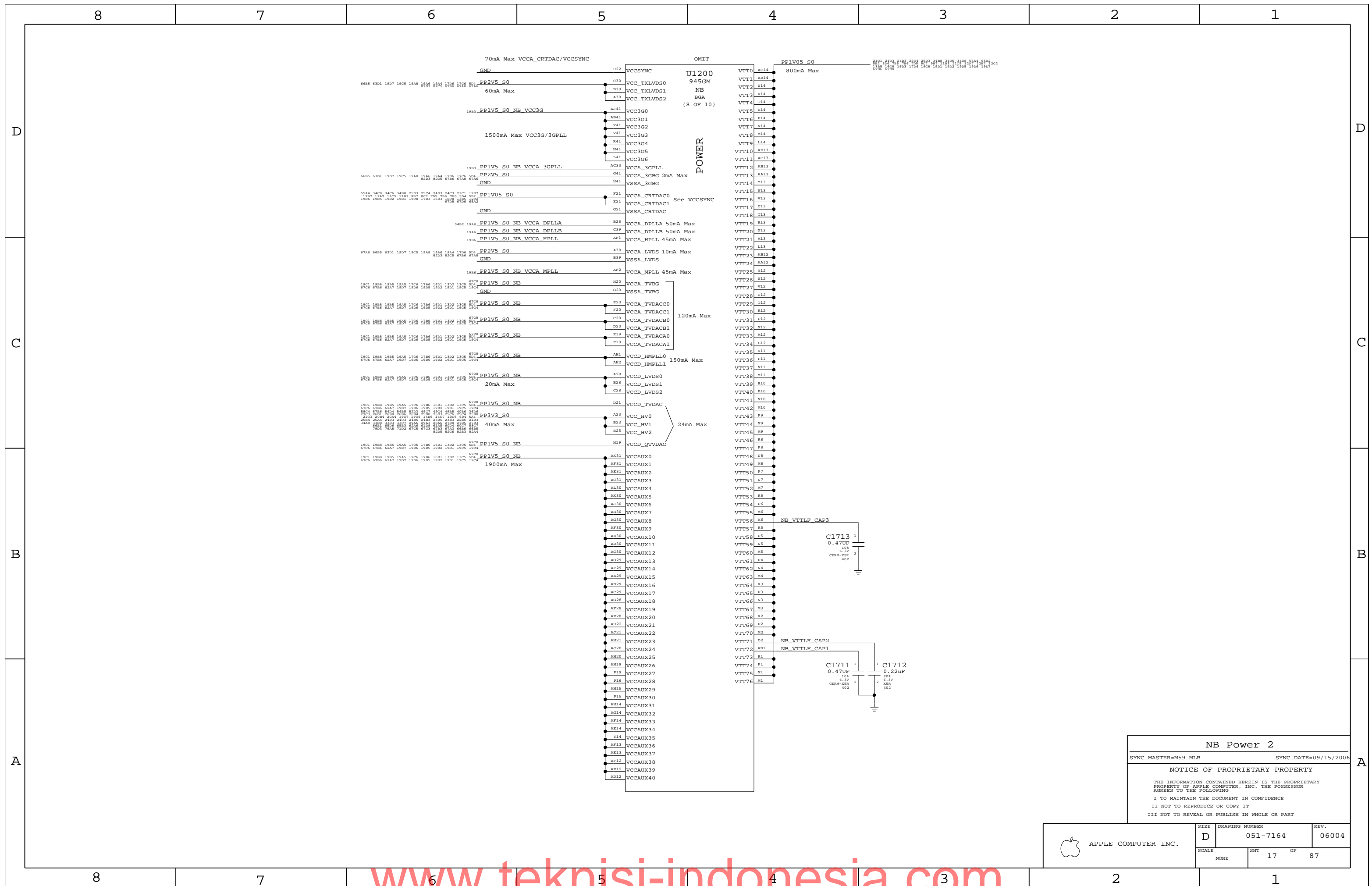
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D

C

B

A

D

C

B

A

AC '07		INTEL HIGH DEFINITION AUDIO	
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR	INTERNAL 20K PD ONLY ENABLED IN S3COLD	
ACZ_RST#	- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE	
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD	
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR	
	- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	
ACZ_SYNC		INTERNAL 20K PD	

SB: 1 OF 4

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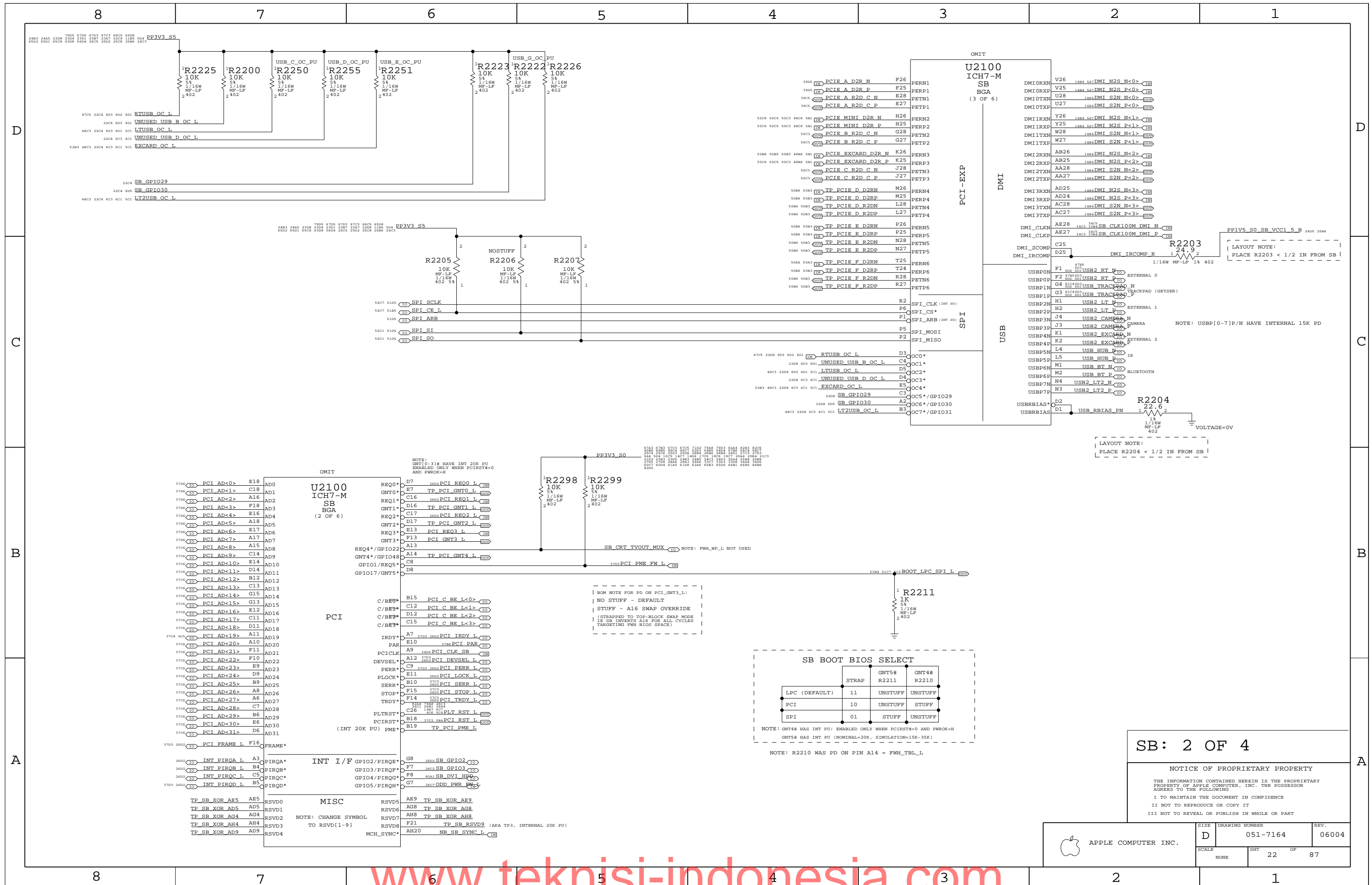
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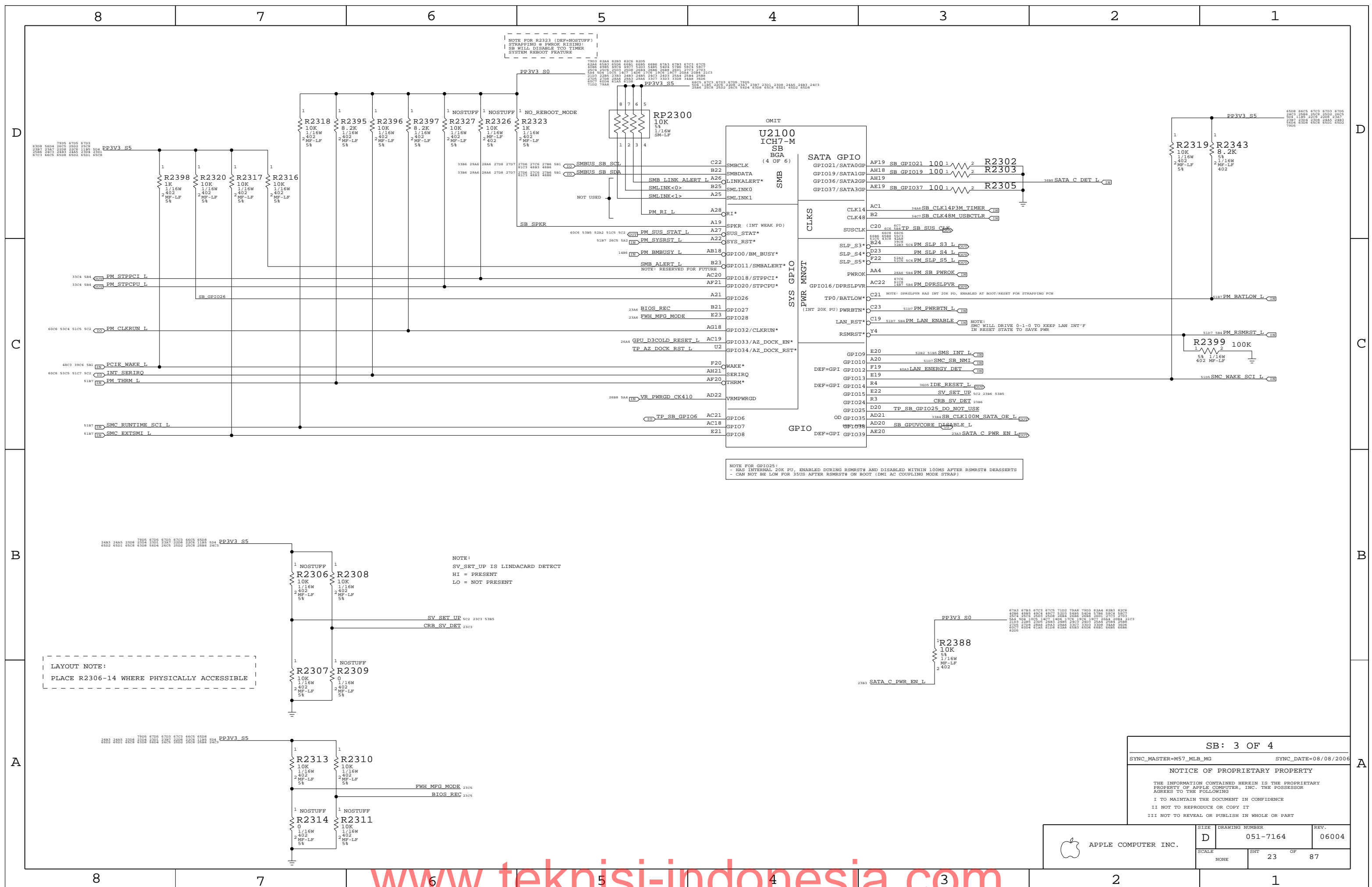
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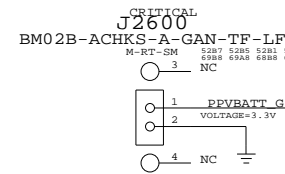




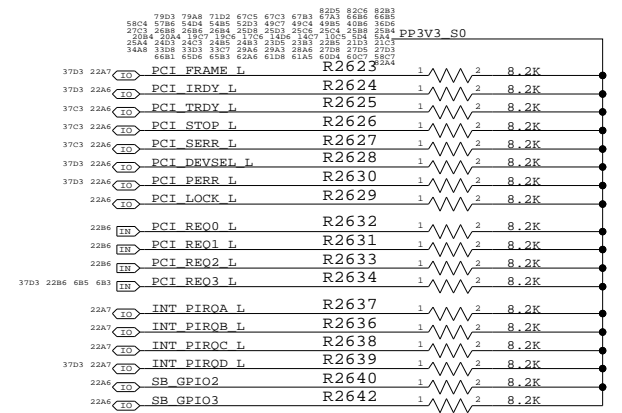
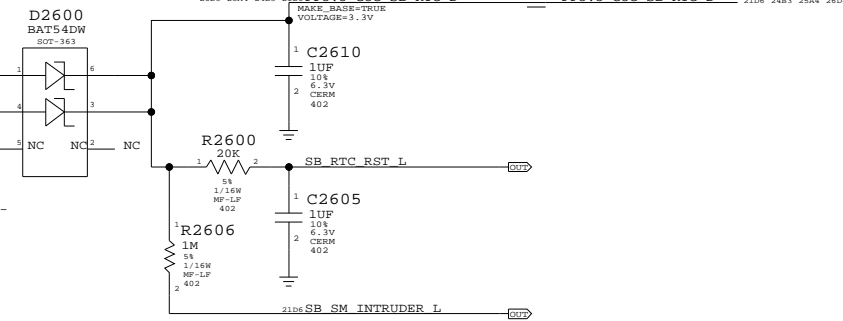








NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



## Platform Reset Connections

Schematic diagram of the SB RTC X1 and X2 circuit. The circuit includes two 10M resistors (R2609) connected to SB\_RTC\_X1 and SB\_RTC\_X2. A 1/16M MF-LP 402 capacitor (R2610) is connected between SB\_RTC\_X1 and SB\_RTC\_X1 R. A Y2600 32.768K SM-2 crystal is connected between SB\_RTC\_X1 and SB\_RTC\_X1 R. Two 12pF capacitors (C2608 and C2609) are connected between SB\_RTC\_X1 and SB\_RTC\_X1 R. The circuit is labeled CRITICAL.

7805 6705 67D3 67C3 66C5 65D8 pp3v3 S5  
 63D8 63B7 62D8 62C8 61D8 61B7 60D8 60B7  
 64D4 64C4 25D2 25C8 25B6 24C3 24B3

R2697<sup>1</sup>  
 100K  
 5%  
 1/16W  
 HP-LF  
 402

ITP  
 R2696  
 1K  
 1/16W  
 HP-LF  
 402

PM SYSRST L  
 MAKE\_BASE=TRUE  
 ODP

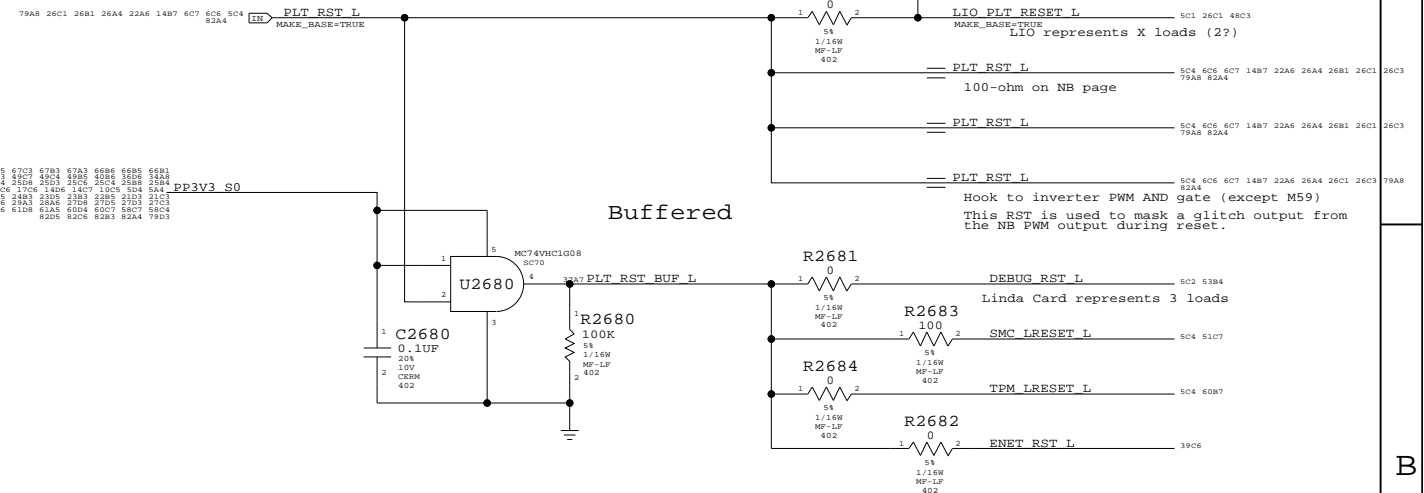
OMIT  
 R2698<sup>1</sup>  
 100K  
 5%  
 1/16W  
 HP-LF  
 402

This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

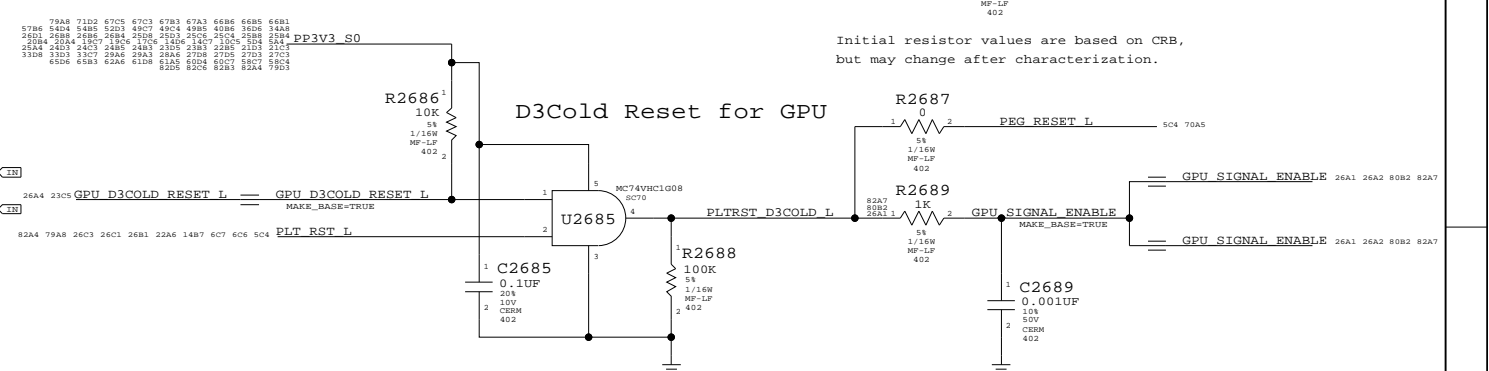
5786	79A8
5811	5828
5836	5844
2084	2084
2534	2083

Silk: "SYS RST"

	79A8	1D12	67C5	67C3	67B3	67A3	66B6	66B5	66B1
5786	54D4	54B5	52D3	49C7	49C4	49B5	40B6	36D6	34A8
26D1	26A8	26B6	26A4	25D8	25D3	25C6	25C4	25B8	25B4
20B4	20A4	19C7	19C6	17C5	14C6	14C7	10C5	5A4	5A4
25A4	24D3	24C3	24B5	24B3	23D5	23B3	22B5	21D3	21C3
31D8	31D3	31C7	29A6	29A3	28A6	27D8	27B5	27C3	27C3
	65D6	65B3	62A6	61D8	61A5	60D4	60C7	58C7	58C4
					82D5	82C6	82B3	82A4	79D3

[illegible]

The schematic diagram illustrates the PP3V3 S0 power supply circuit. It features a central U2601 IC, which is a voltage regulator. The input to the IC is connected to the PM\_SB PWROK signal through a 10K resistor (R2612). The output of the IC is connected to the ALL SYS PWRGD signal through another 10K resistor (R2622). A feedback network consisting of a 1.8K resistor (R2611) and a 10V capacitor (C2607) is connected between the output and the IC's feedback pin. The IC is also connected to ground at its reference pin. The circuit is powered by a 5V source, which is connected to the IC's enable pin and the positive terminal of the feedback network. The negative terminal of the feedback network is connected to ground.



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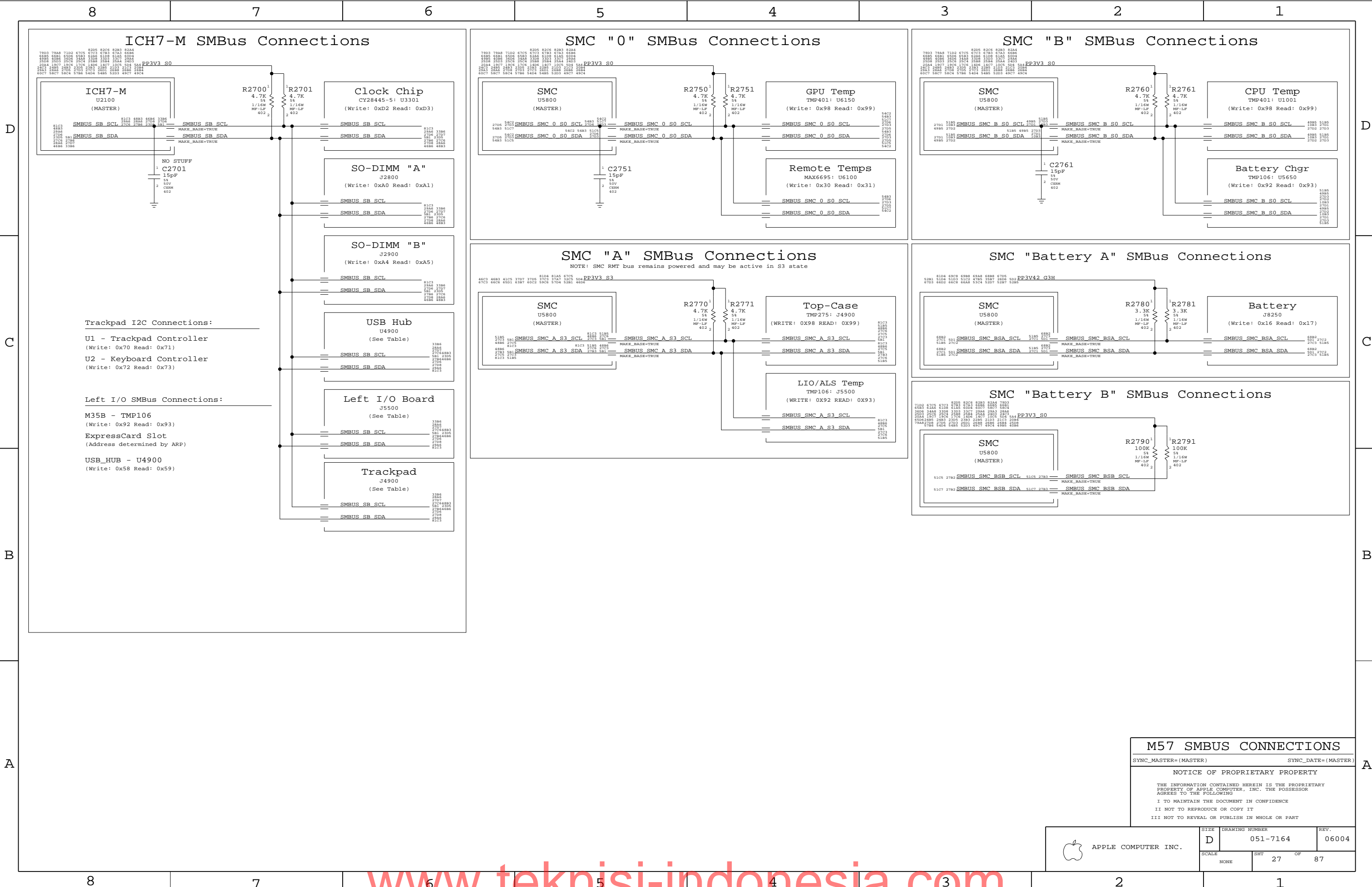
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M57 SMBUS CONNECTIONS

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Power aliases required by this page:

- =PP1V8\_S3\_MEM
- =PPSPD\_S0\_MEM (2.5V ~ 3.3V)

---

Signal aliases required by this page:

- =I2C\_SODIMMA\_SCL
- =I2C\_SODIMMA\_SDA

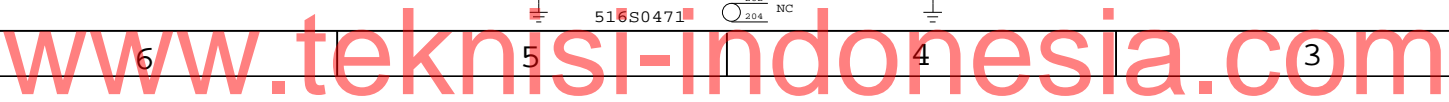
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NOTE: This page does not supply VREF.  
The reference voltage must be provided  
by another page.



29D6 29D3 29B2 28D4 28D3 19D7 16B6 14C2 5D4 5B2 67B8 67B6 64C1 64A6 37B2 32C6 31C5

PP1VS S3

1 C2808 10UF 20% 6.3V X5R 603

1 C2809 10UF 20% 6.3V X5R 603

1 C2810 10UF 10% 6.3V CERM 402

1 C2811 10UF 10% 6.3V CERM 402

1 C2812 10UF 10% 6.3V CERM 402

1 C2813 10UF 10% 6.3V CERM 402

1 C2814 10UF 10% 6.3V CERM 402

1 C2815 10UF 10% 6.3V CERM 402

1 C2816 10UF 10% 6.3V CERM 402

1 C2817 10UF 10% 6.3V CERM 402


1 C2818 10UF 10% 6.3V CERM 402

1 C2819 10UF 10% 6.3V CERM 402

1 C2820 10UF 10% 6.3V CERM 402

1 C2821 10UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector A	
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## Page Notes

Power aliases required by this page:

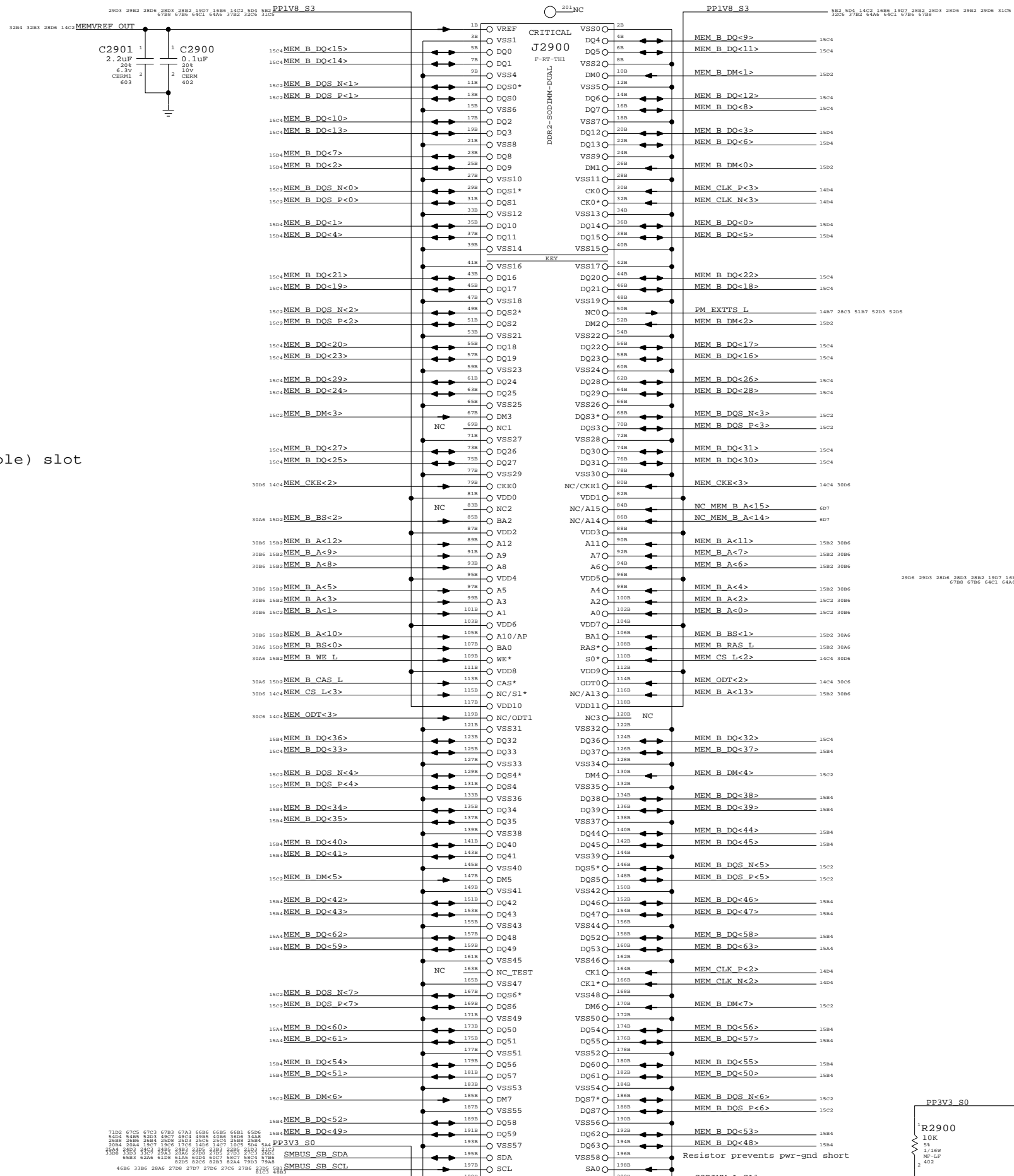
```
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)
```

Signal aliases required by this page:

- =I2C\_SODIMMB\_SCL
- =I2C\_SODIMMB\_SDA

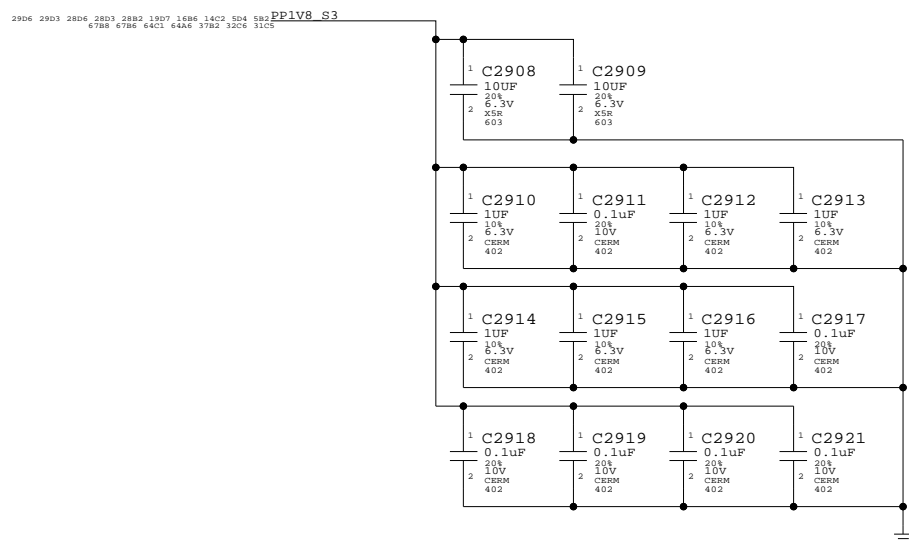
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## DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

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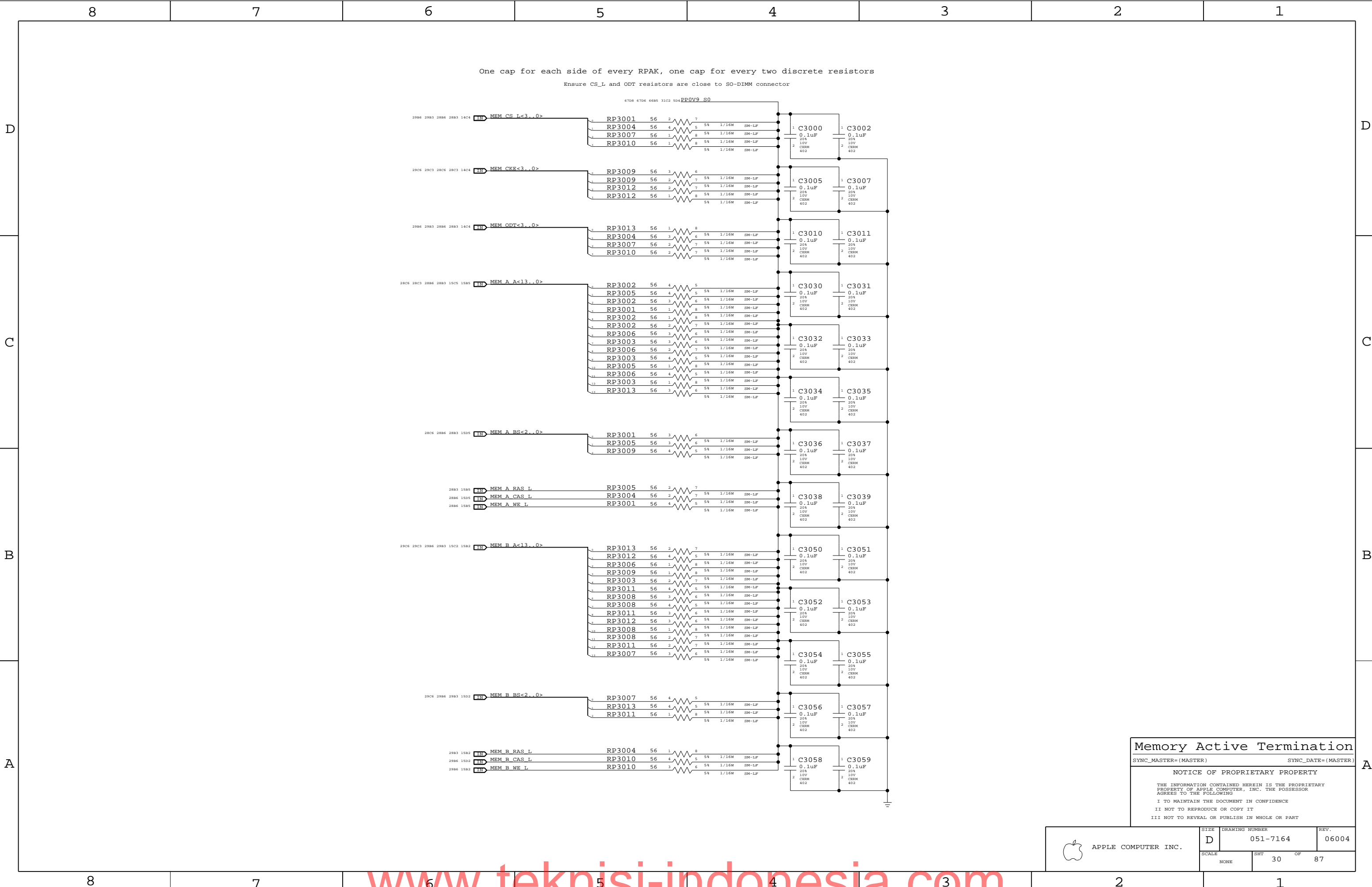
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Memory Active Termination

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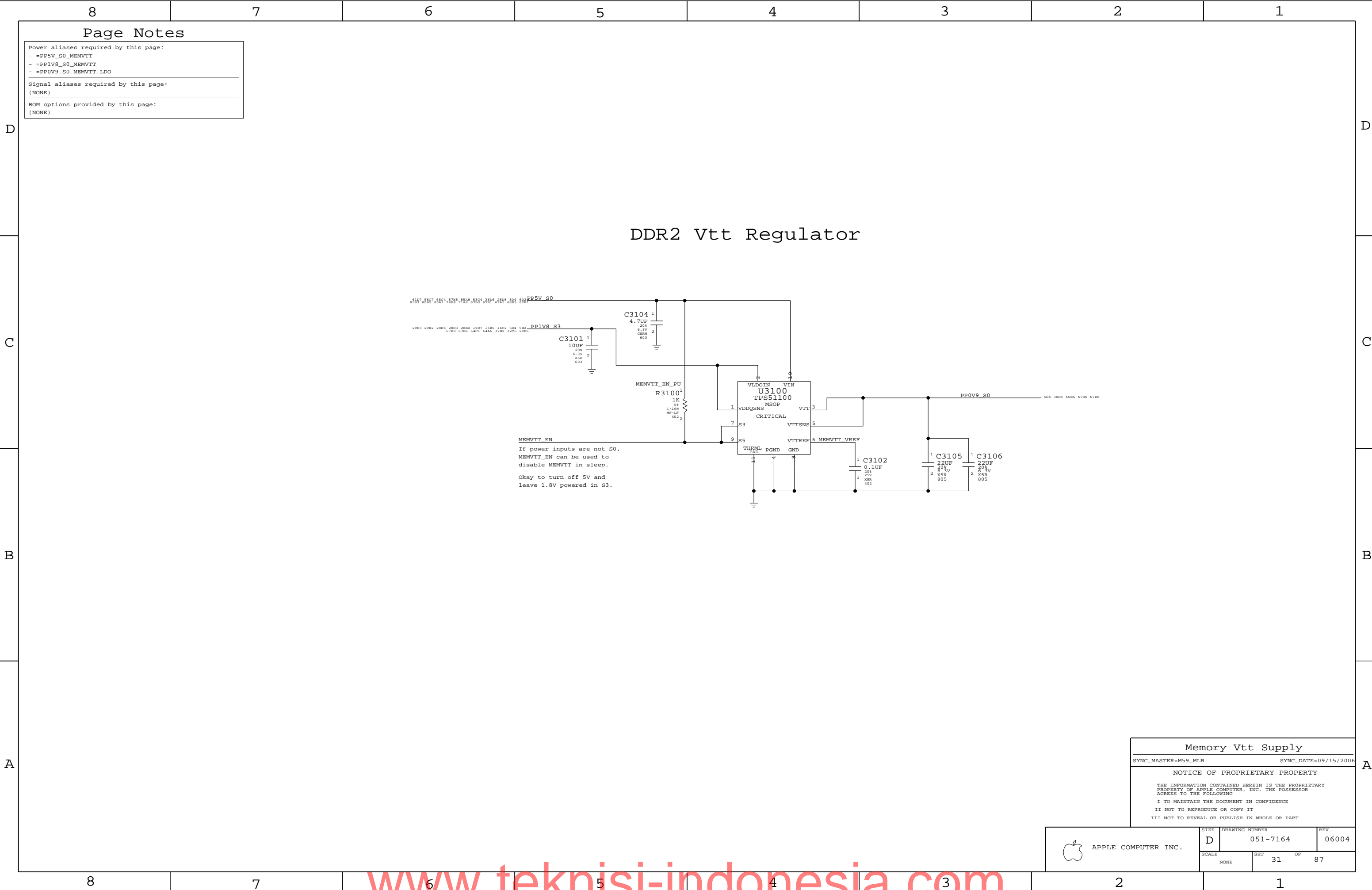
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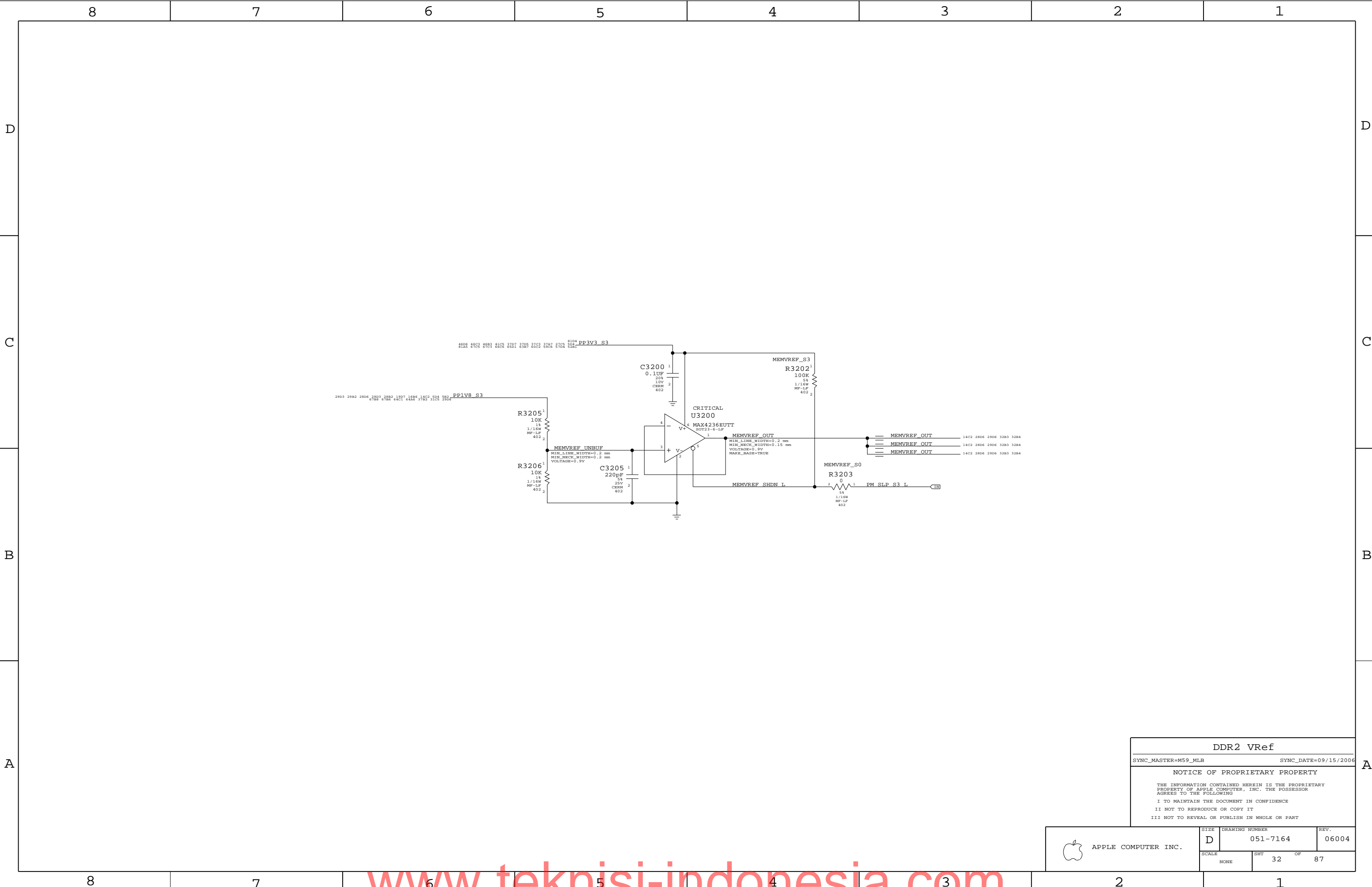
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DDR2 VRef

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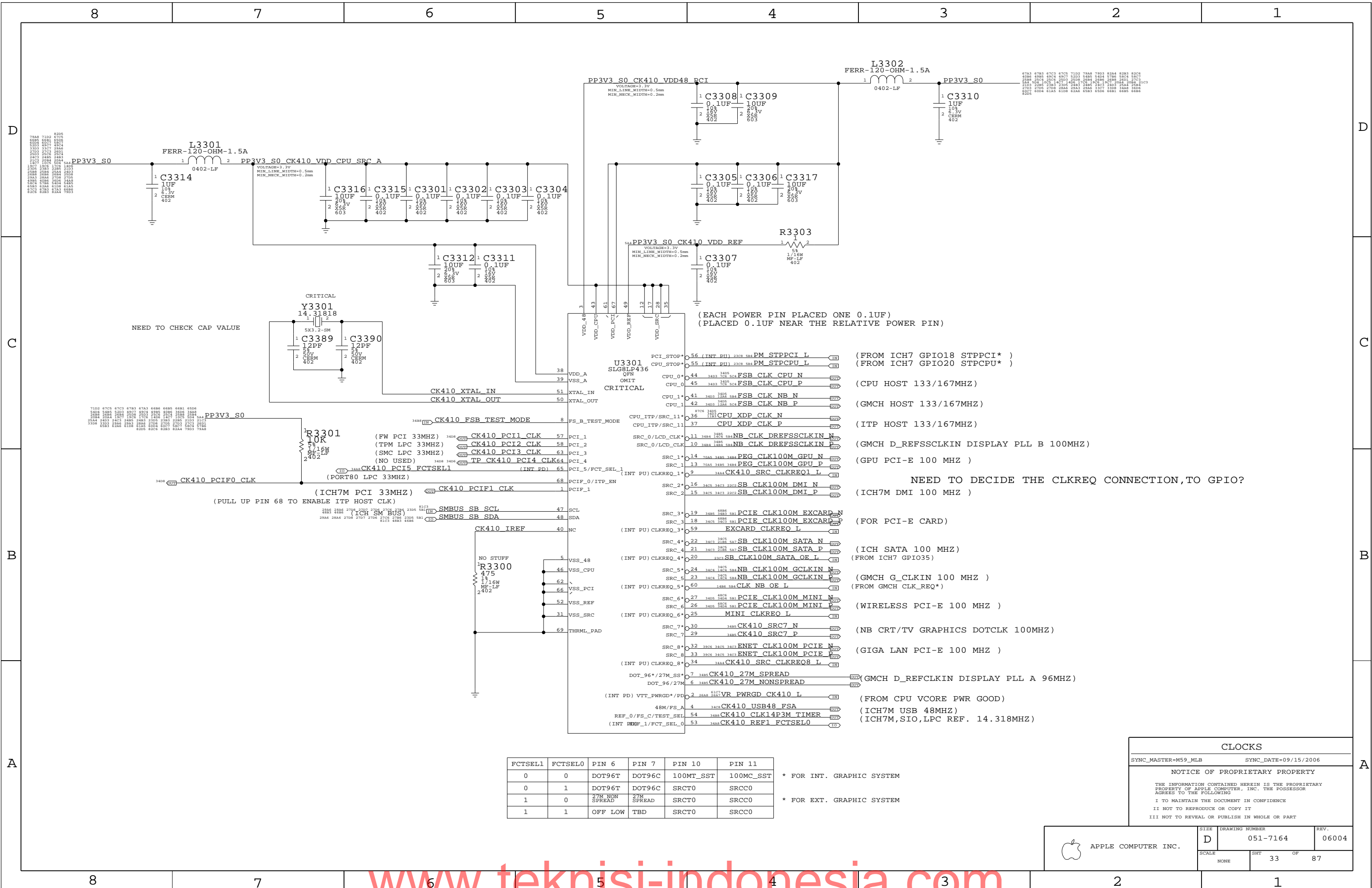
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FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

\* FOR INT. GRAPHIC SYSTEM

\* FOR EXT. GRAPHIC SYSTEM

CLOCKS

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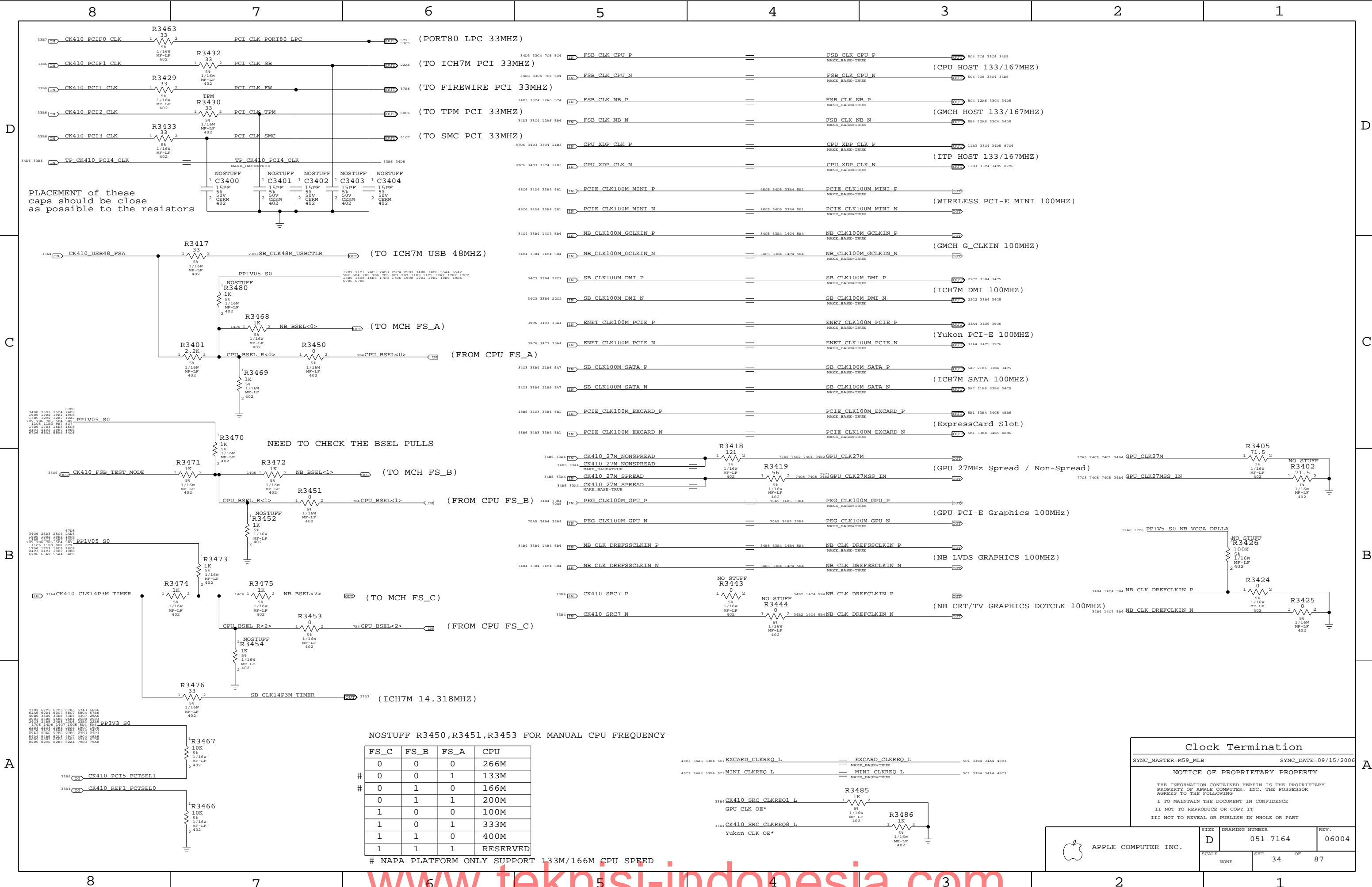
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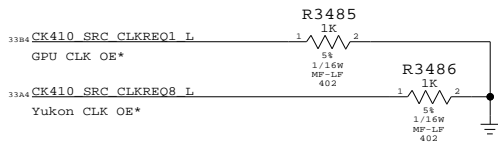
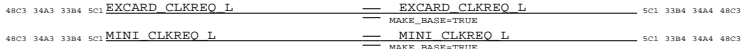
PLACEMENT of these caps should be close as possible to the resistors

NEED TO CHECK THE BSEL PULLS

NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
#	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
#	0	1	1	200M
#	1	0	0	100M
#	1	0	1	333M
#	1	1	0	400M
#	1	1	1	RESERVED

# NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED



Clock Termination

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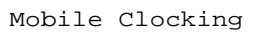
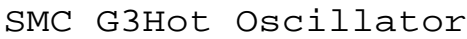
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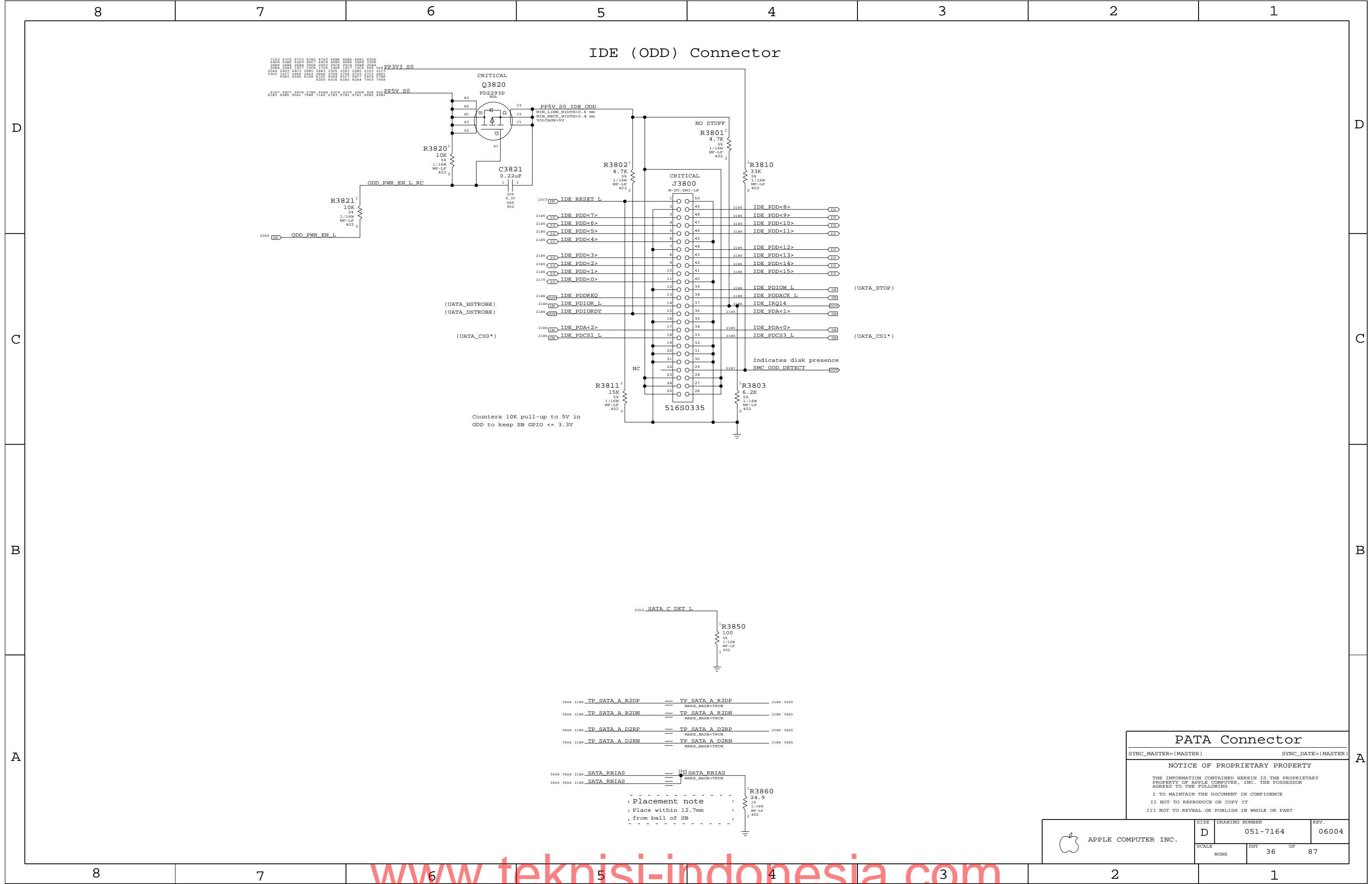
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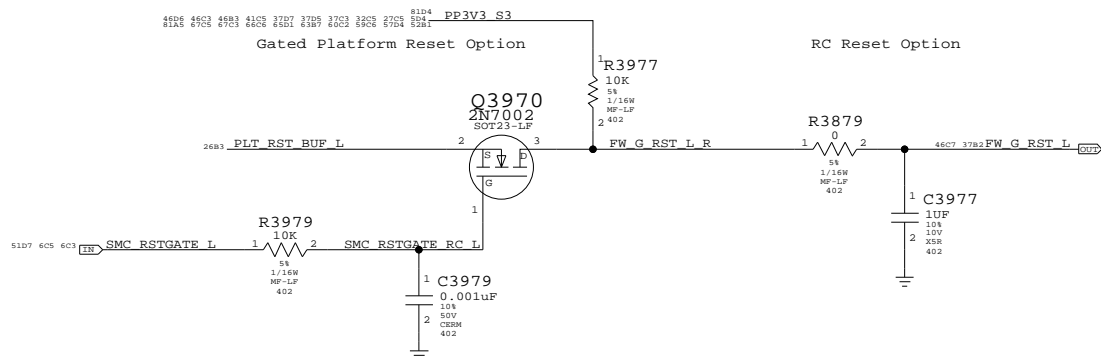
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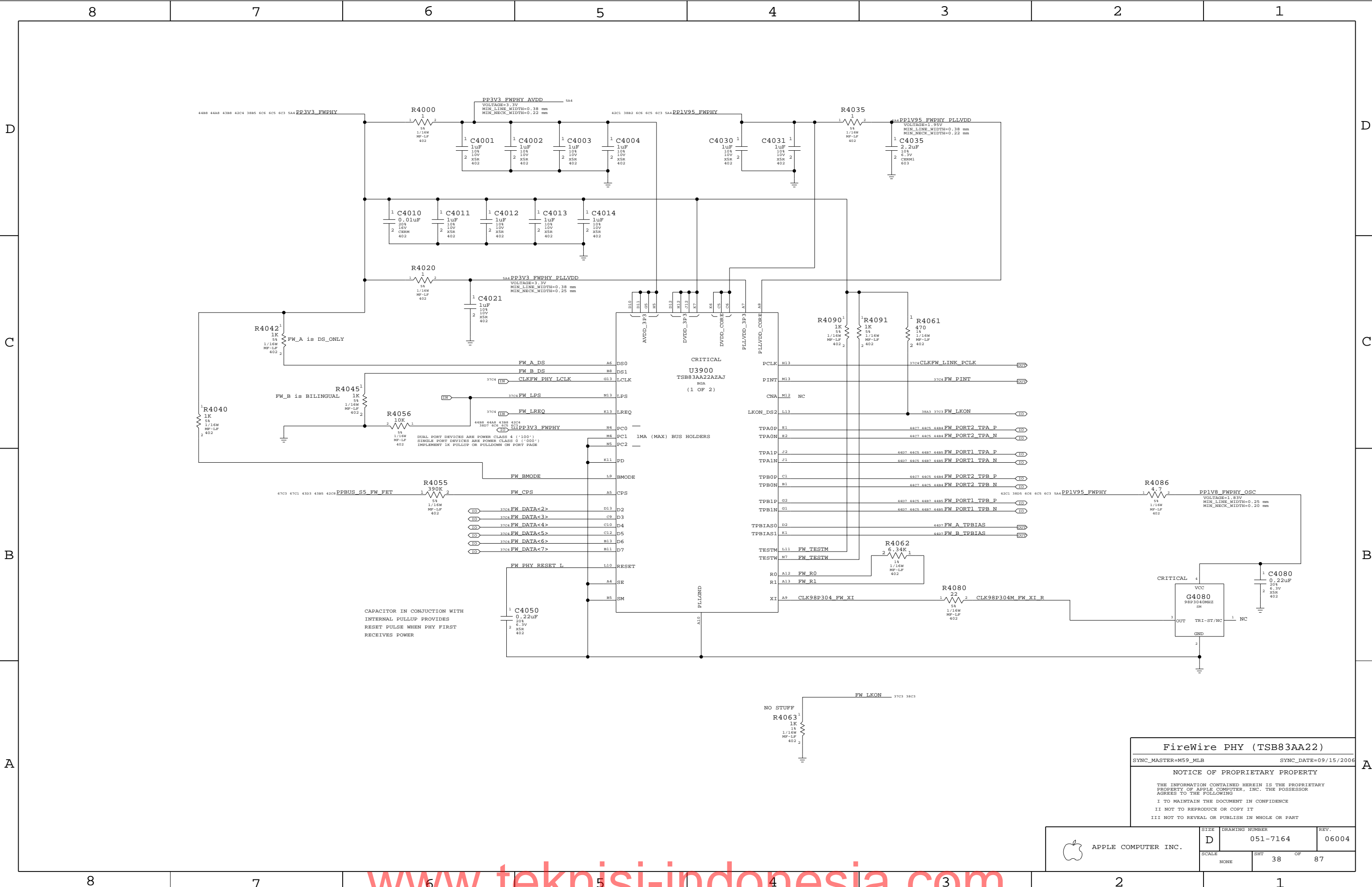
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FireWire PHY (TSB83AA22)

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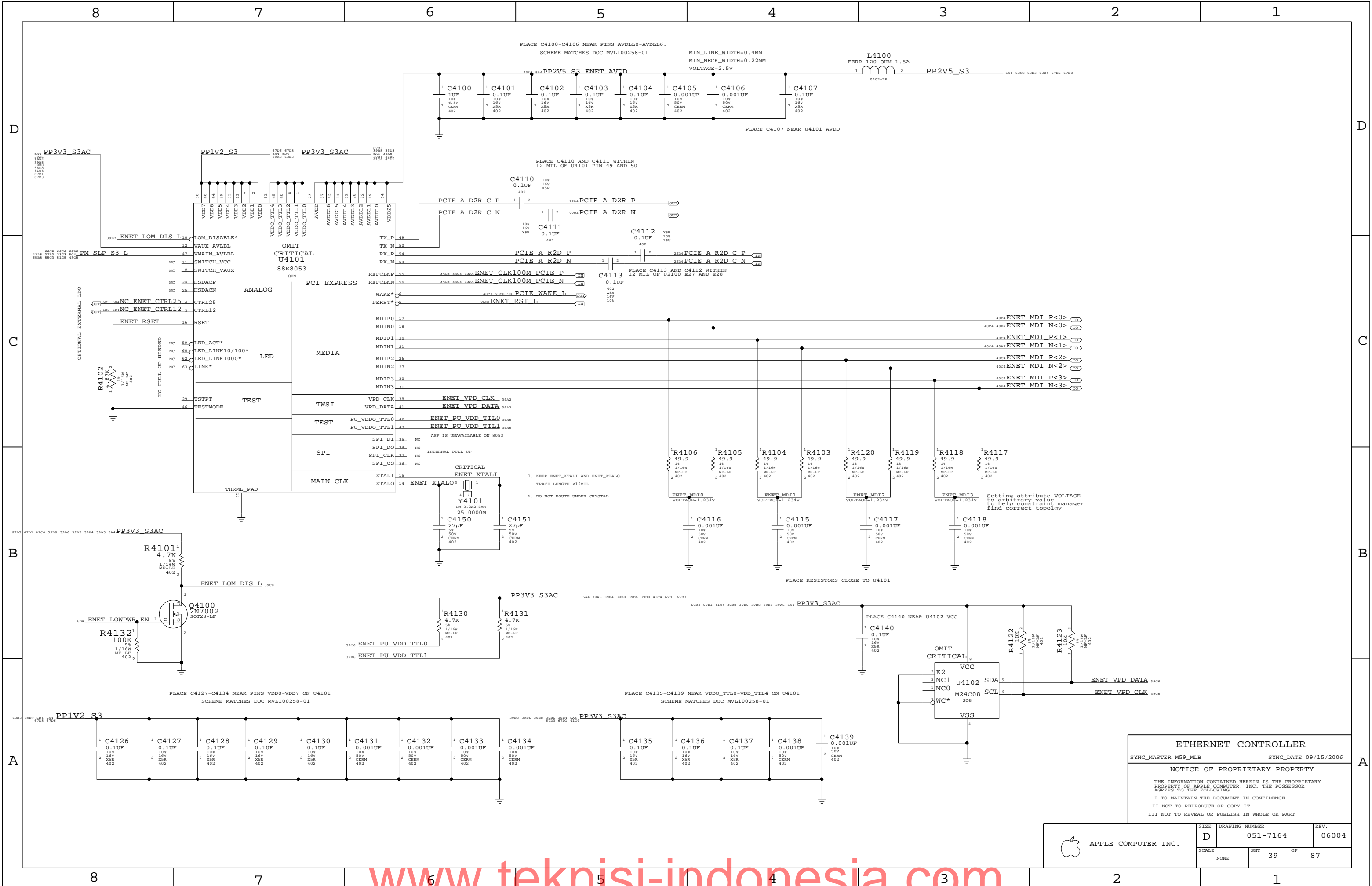
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ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL		
PROVIDED	ENETCONN	ENET_100D	ENETCONN_P<0>	40D3
	ENETCONN	ENET_100D	ENETCONN_N<0>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<1>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<1>	40C3
BY	ENETCONN	ENET_100D	ENETCONN_P<2>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<2>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<3>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<3>	40B3
ETHERNET	ENETCONN	ENET_100D	ENETCONN_P<0>	40D3
PHY	ENETCONN	ENET_100D	ENETCONN_N<0>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<1>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<1>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<2>	40C3

## Page Notes

Power aliases required by this page:

- =PP2V5\_ENET  
- =GND\_CHASSIS\_ENET

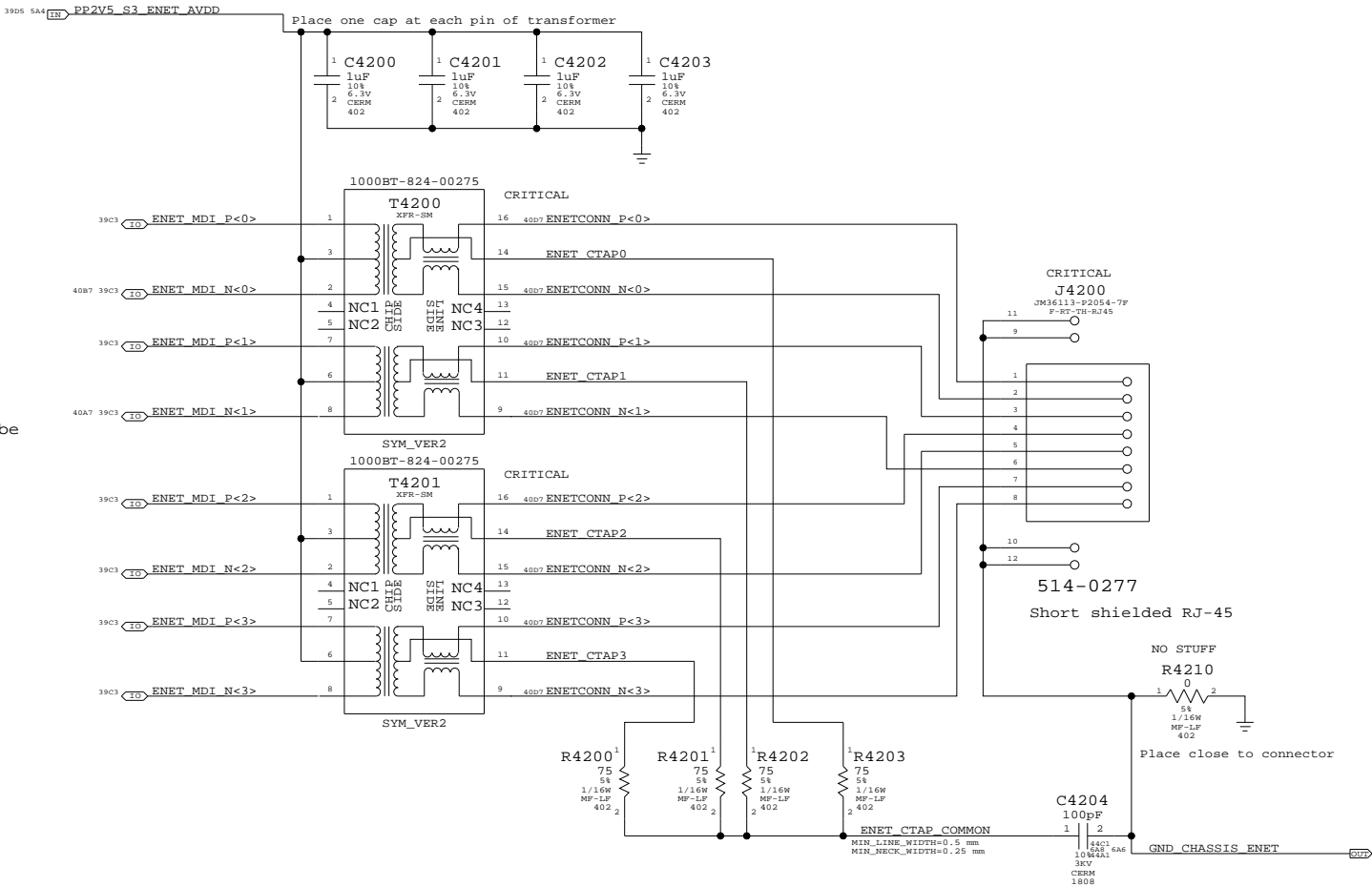
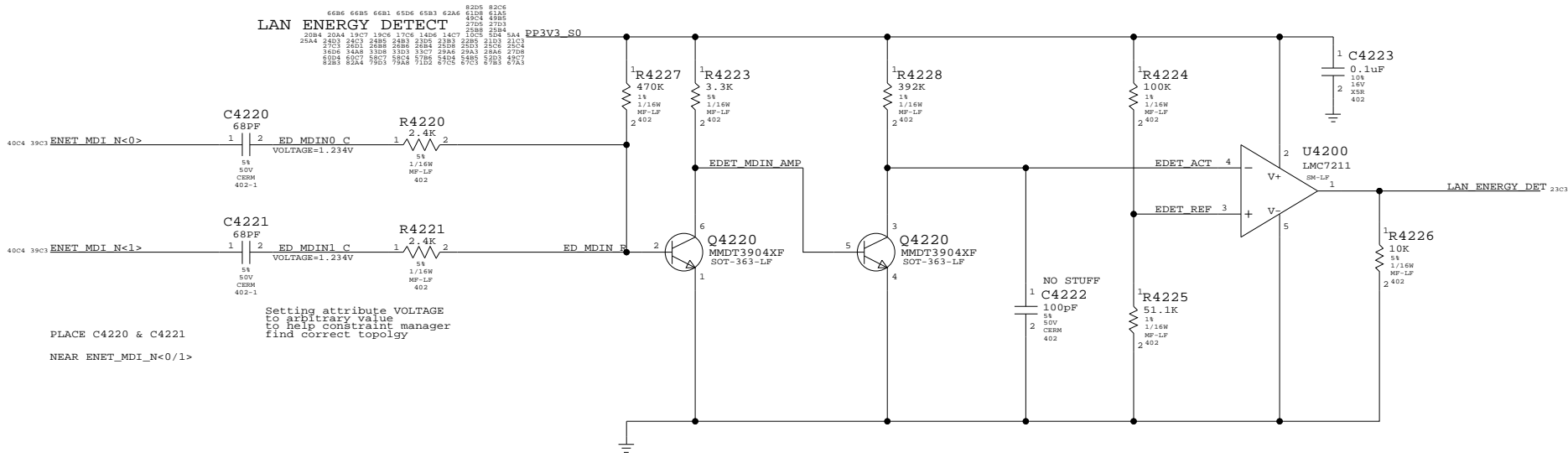
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

Transformers should be mirrored on opposite sides of the board



## Ethernet Connector

SYNC\_MASTER=M59\_MLB SYNC\_DATE=09/15/2006

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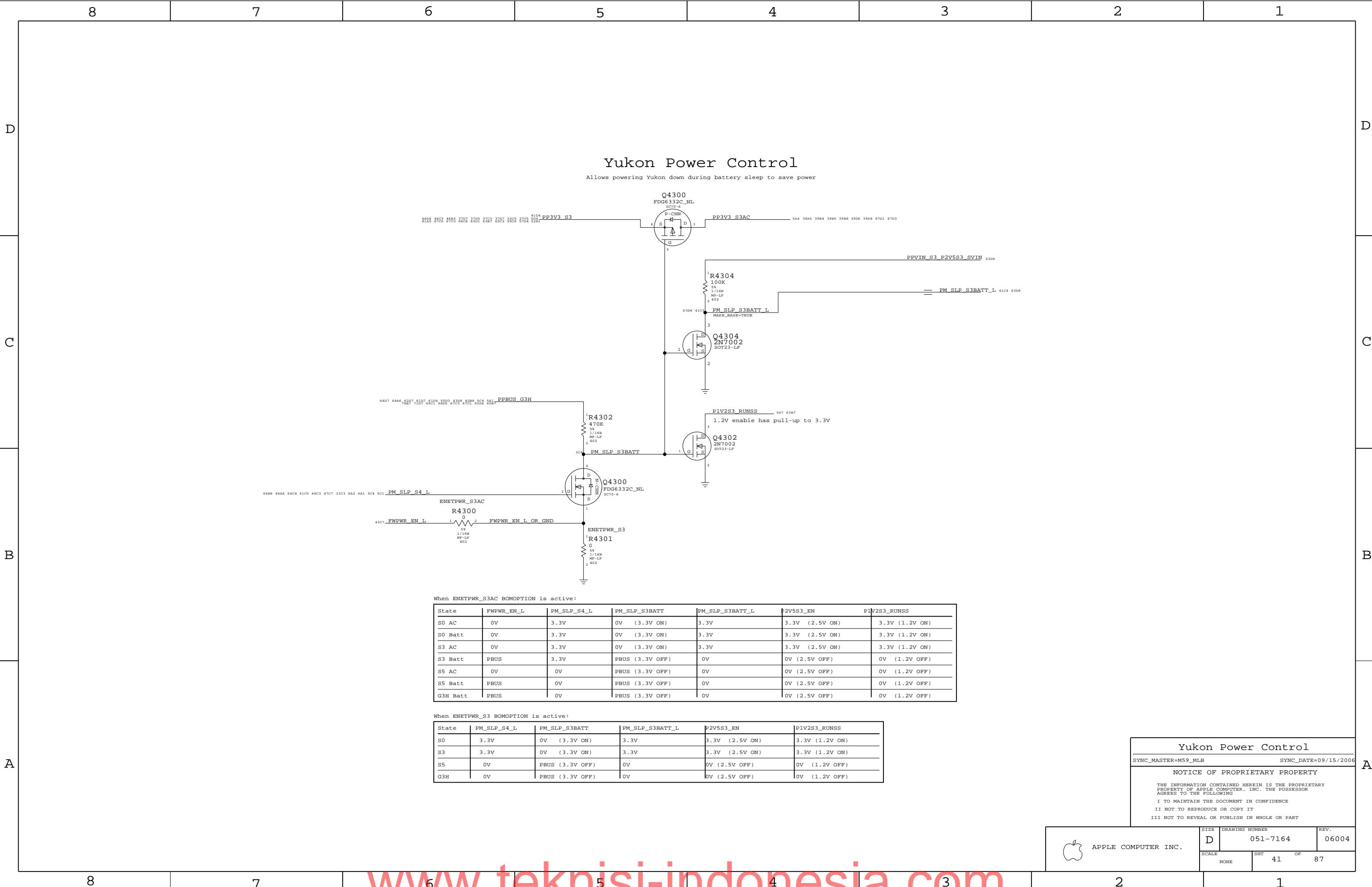
II NOT TO REPRODUCE OR COPY IT

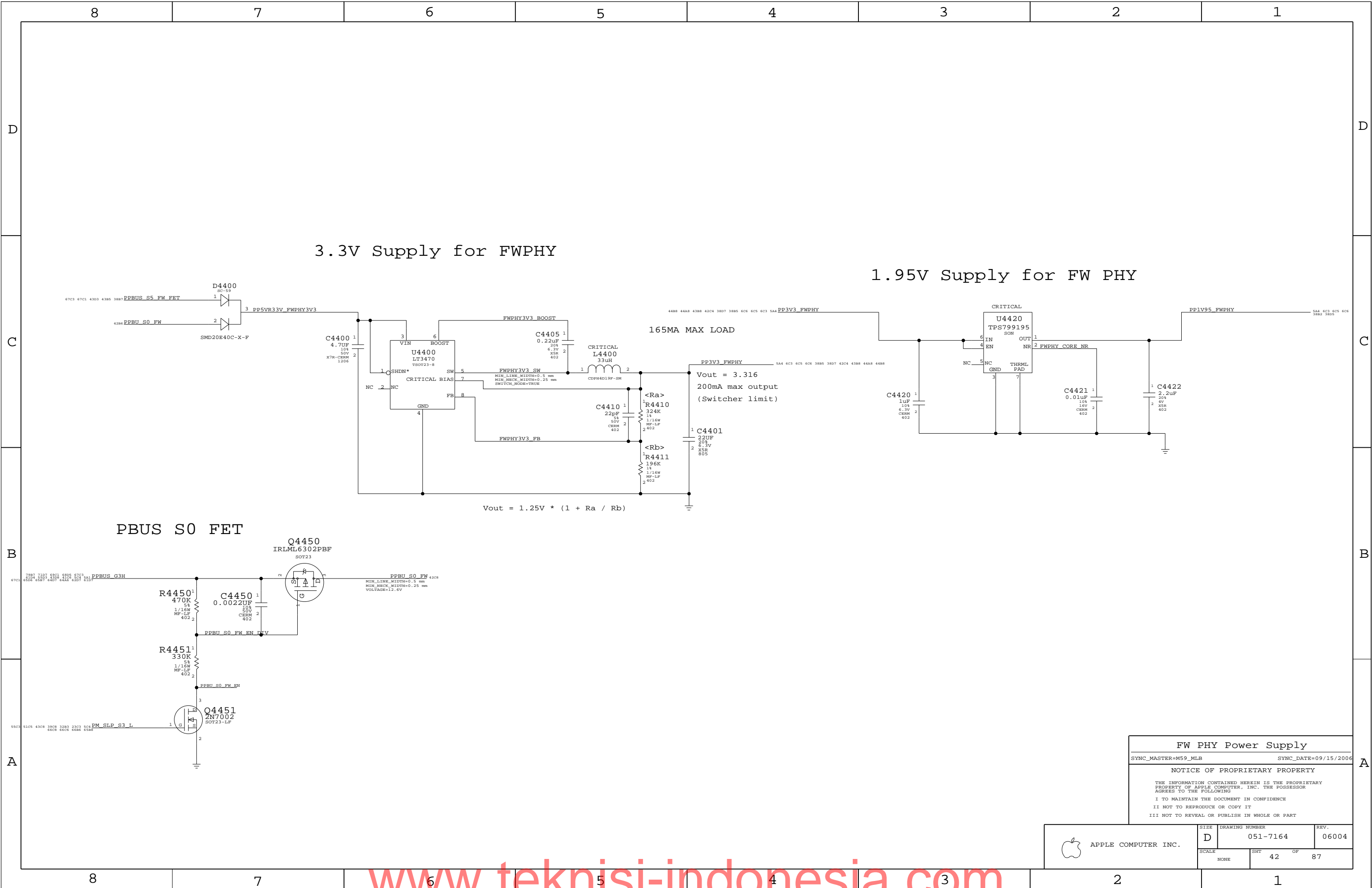
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

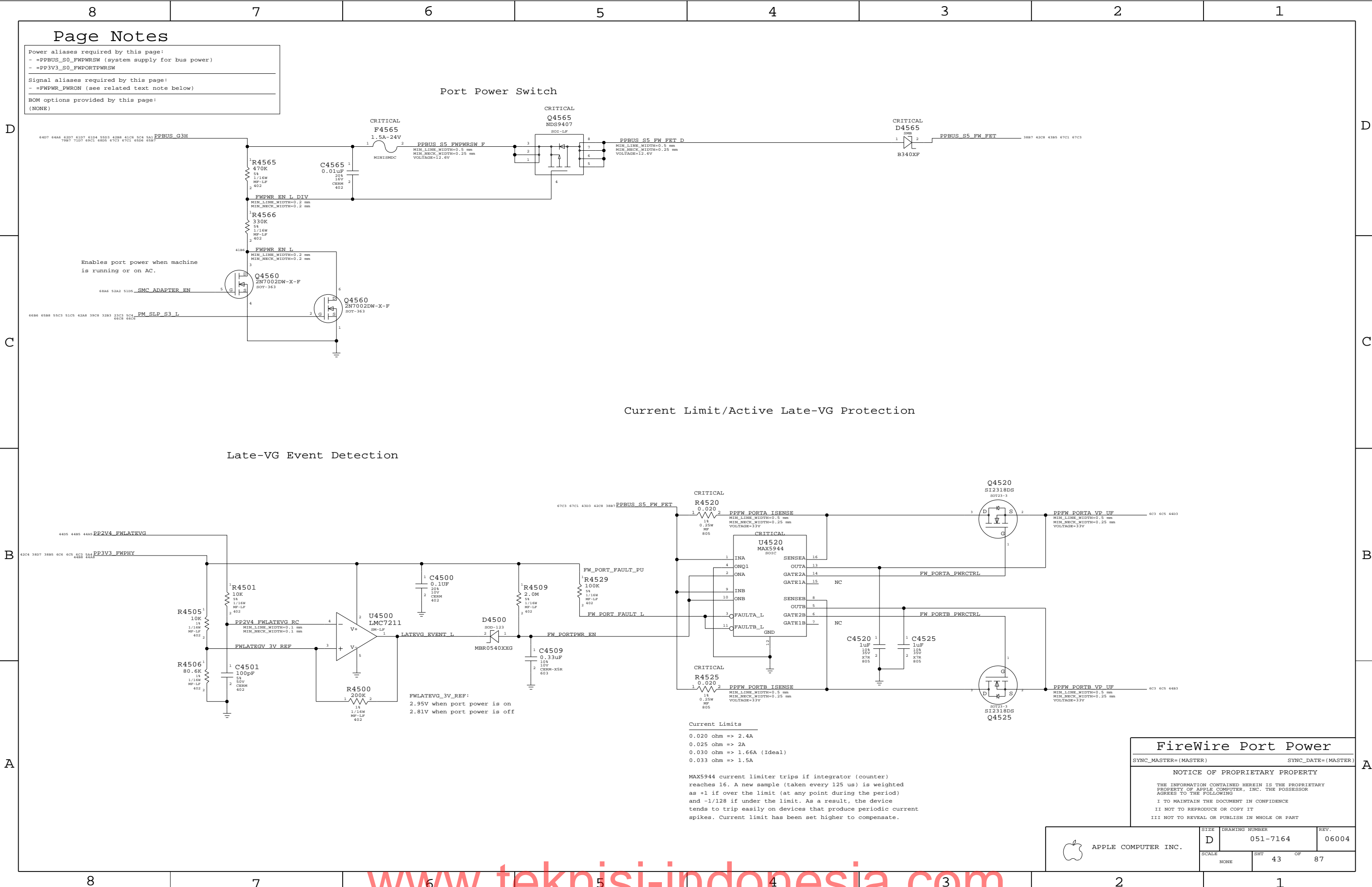


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	40	87









AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

Power aliases required by this page:

- =PPFW\_PORT1
- =PP3V3\_S5\_FWLATEVG
- =GND\_CHASSIS\_FW\_PORT1

---

Signal aliases required by this page:

(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

---

BOM options provided by this page:

(NONE)

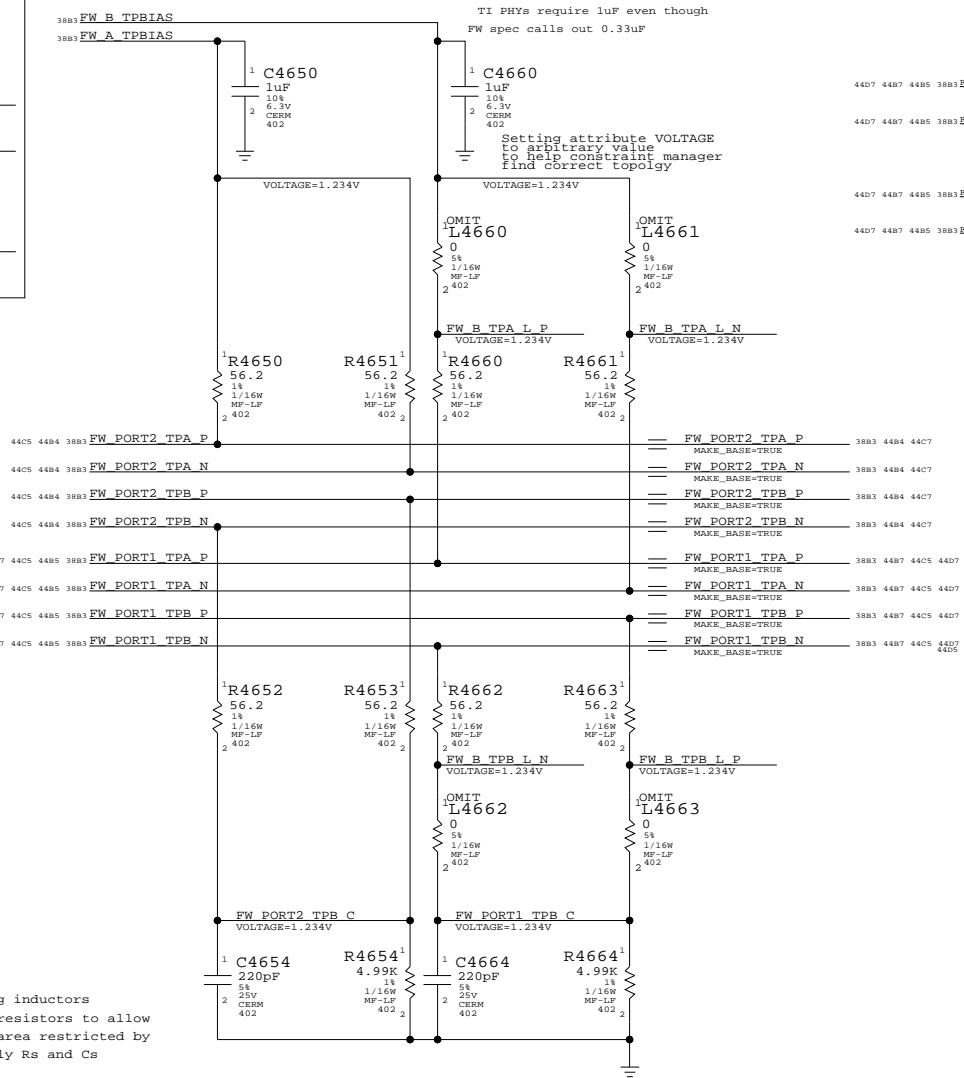
---

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

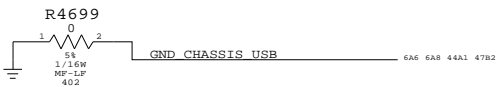
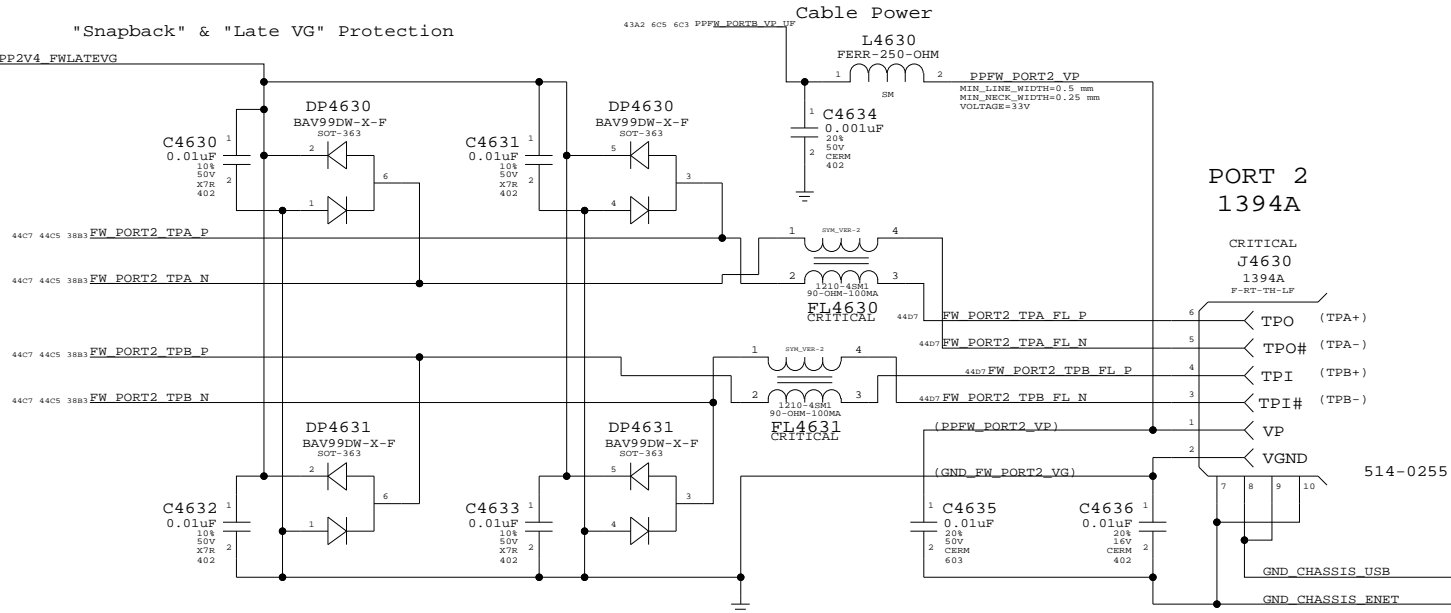
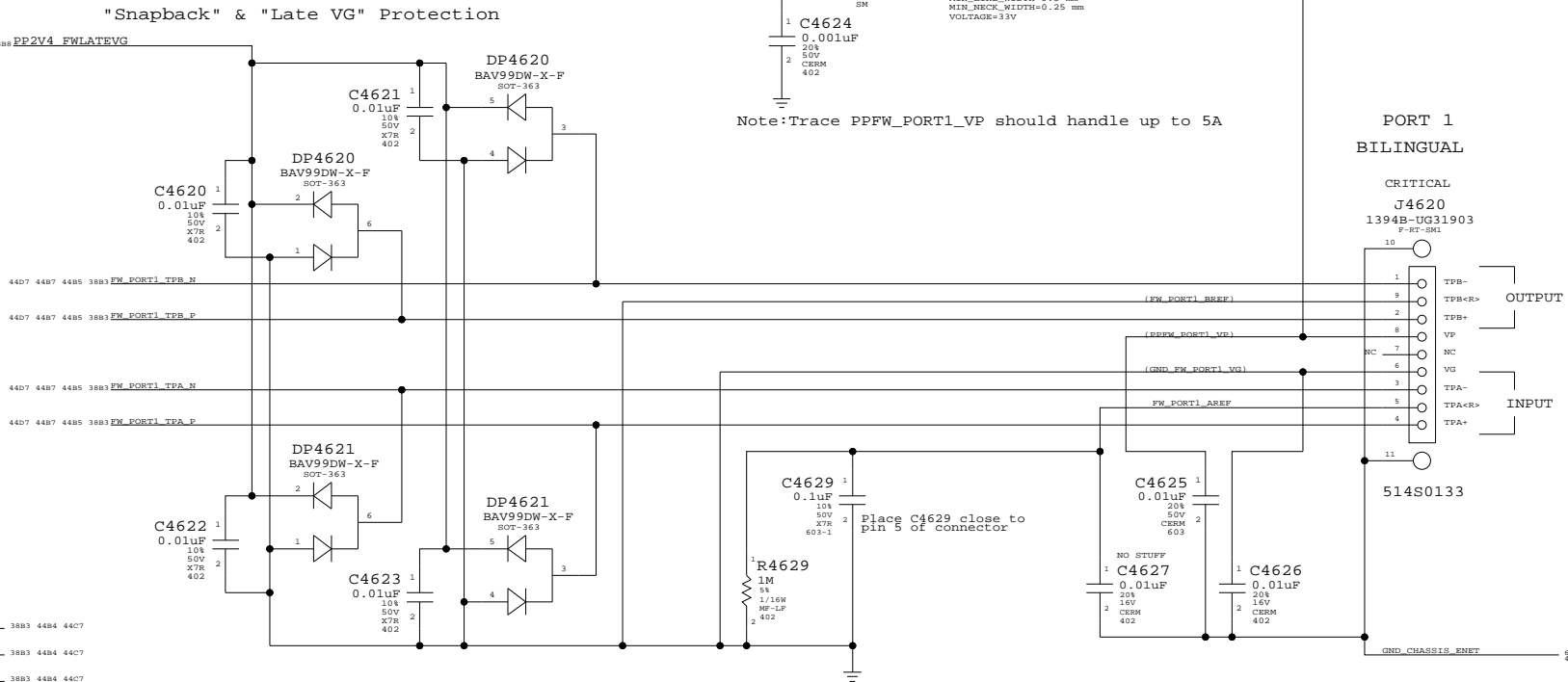
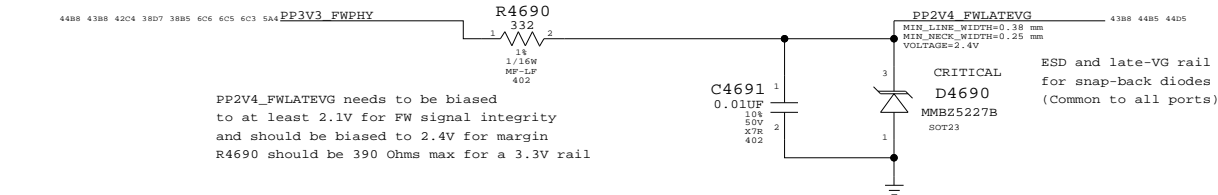
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1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Place close to FireWire PHY



## Late-VG Protection Power



```

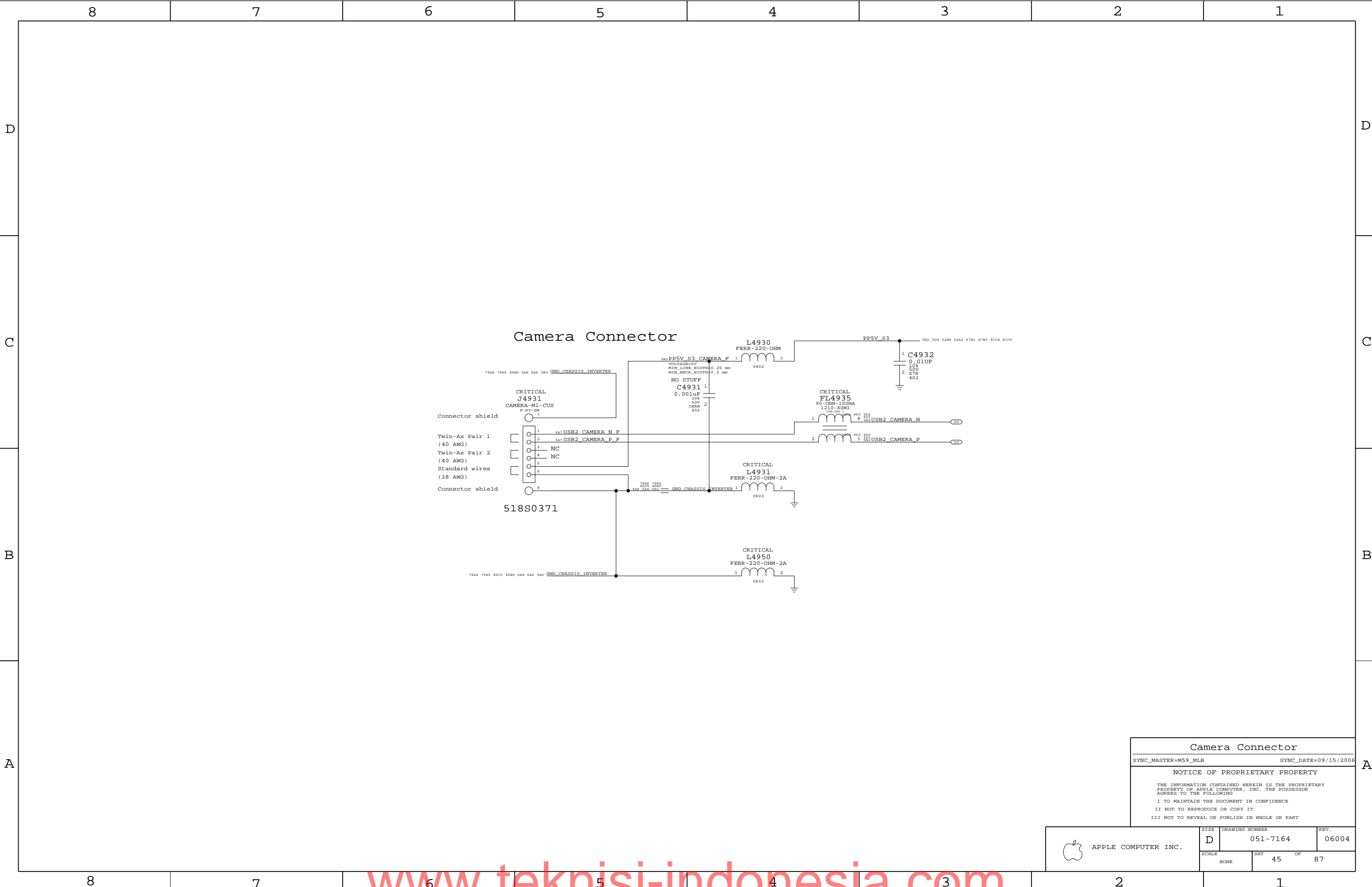
FireWire Ports
SYNCH_MASTER=M59_MLB                               SYNCH_DATE=06/27/2006
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SIZE D	DRAWING NUMBER 051-7164	REV. 06004
SCALE NONE	SHT 44	OF 87



Camera Connector

SYNC\_MASTER=M59\_MLB

SYNC\_DATE=09/15/2006

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	D	051-7164	06004
SCALE		SHT	OF
NONE		45	87



D

C

B

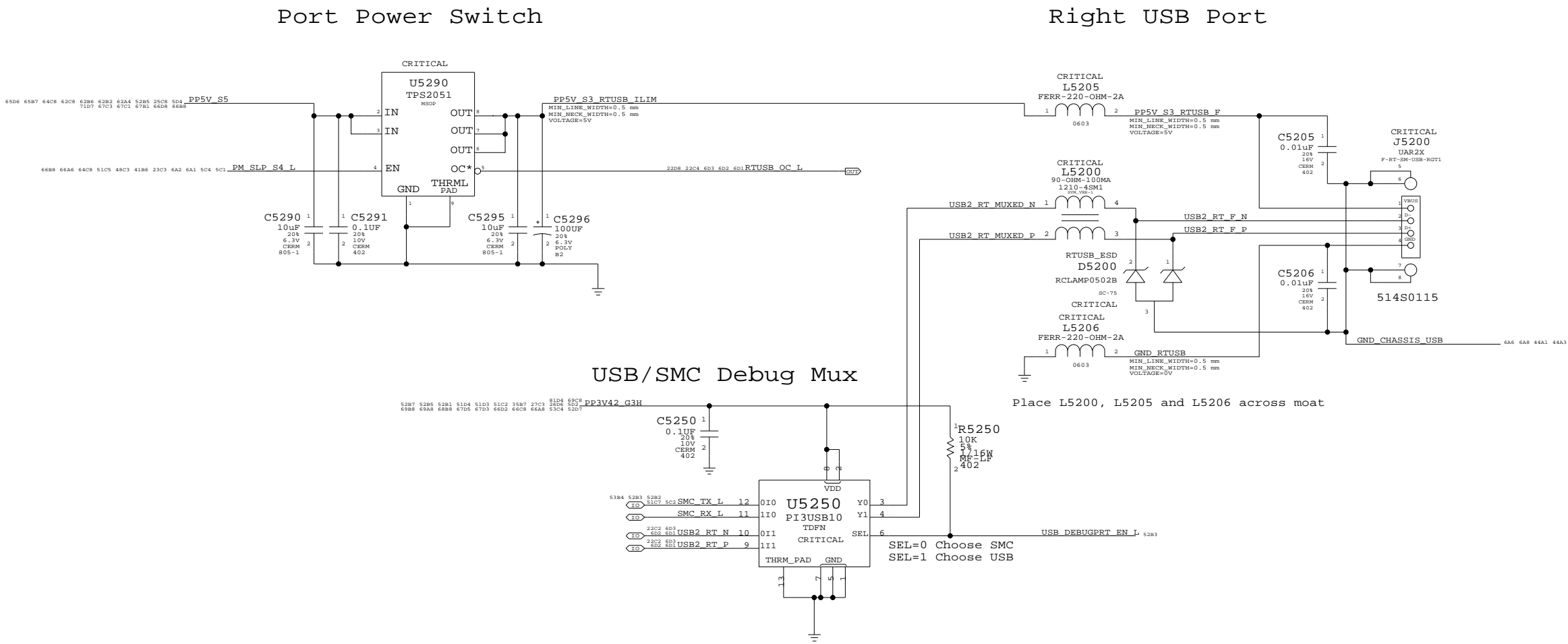
A

D

C

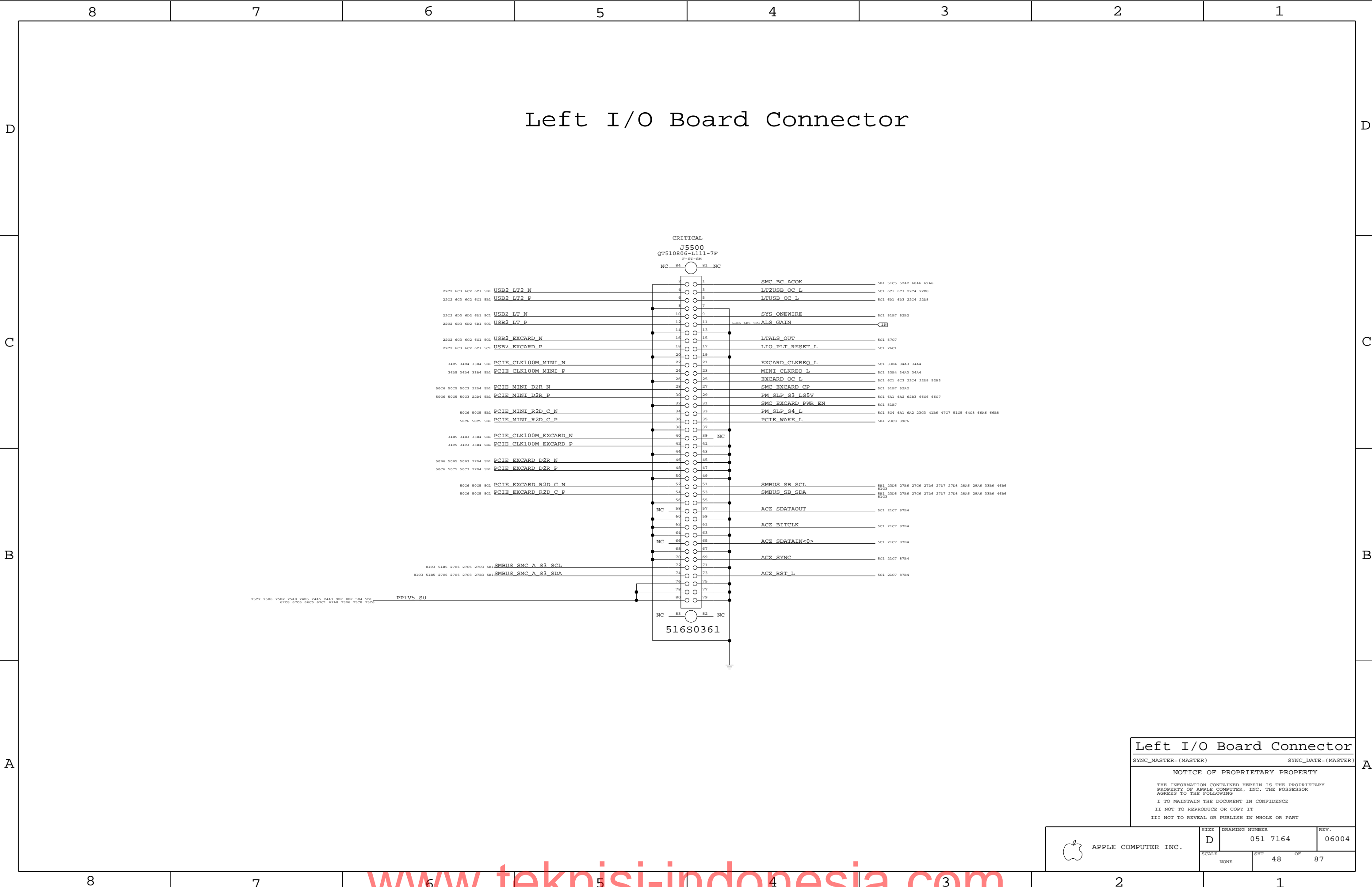
B

A



External USB Connector		
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	D	051-7164	06004
SCALE		SHT	OF
NONE		47	87



Left I/O Board Connector

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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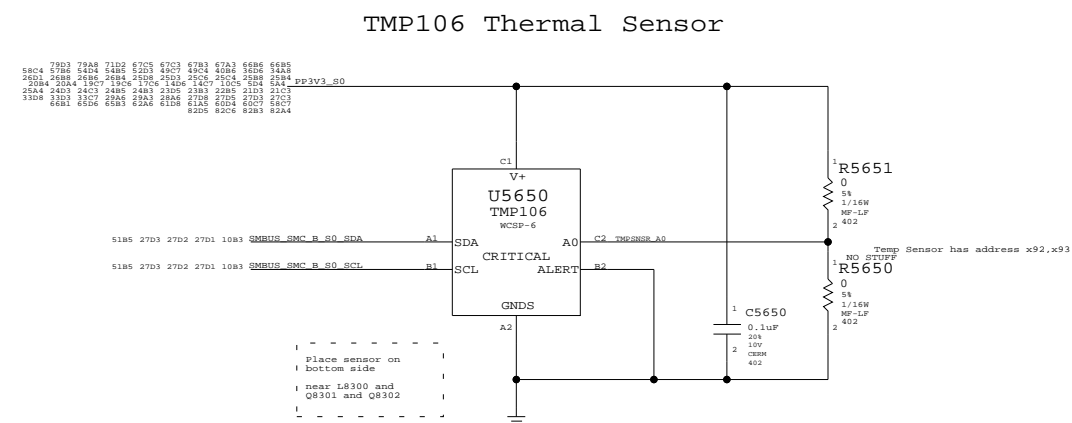
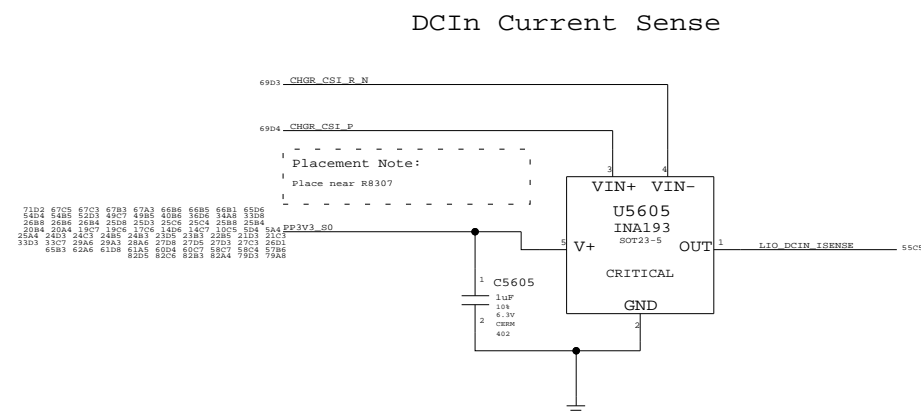
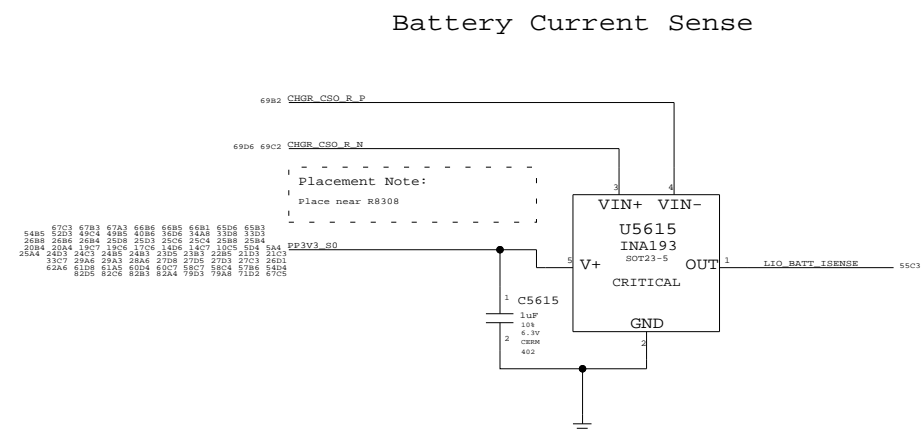
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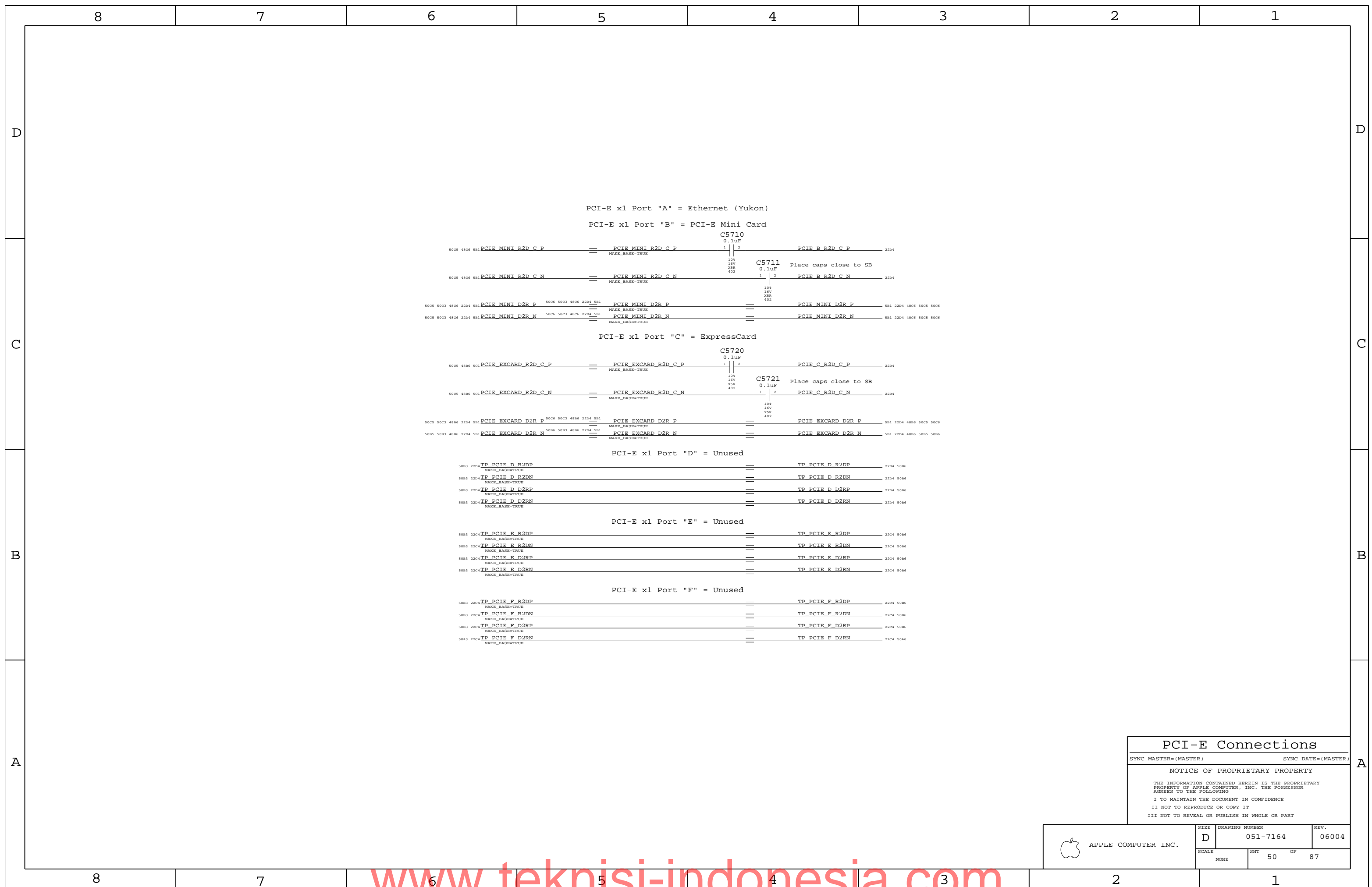
APPLE COMPUTER INC.

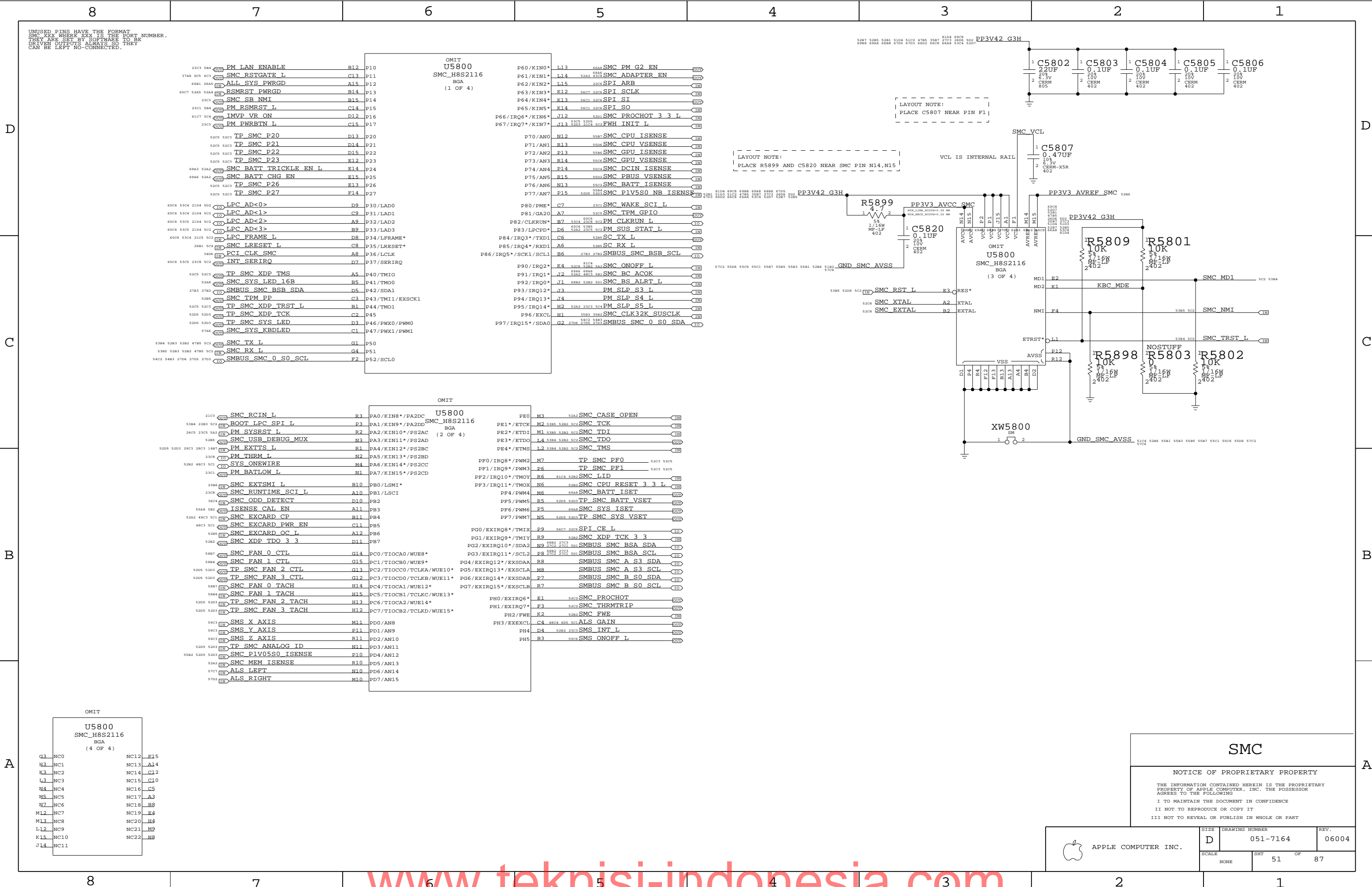
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SCALE	SHT	OF
NONE	48	87

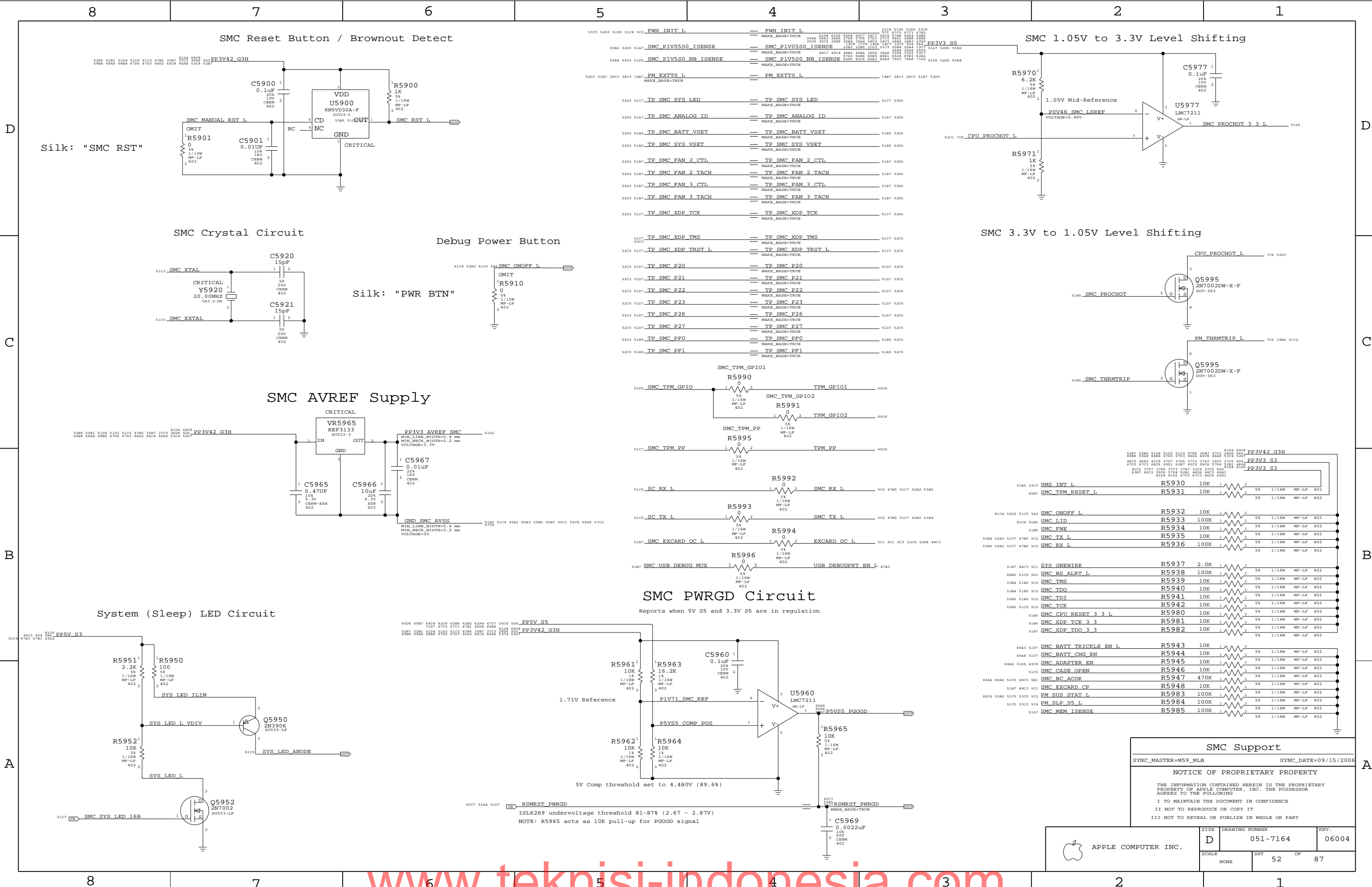


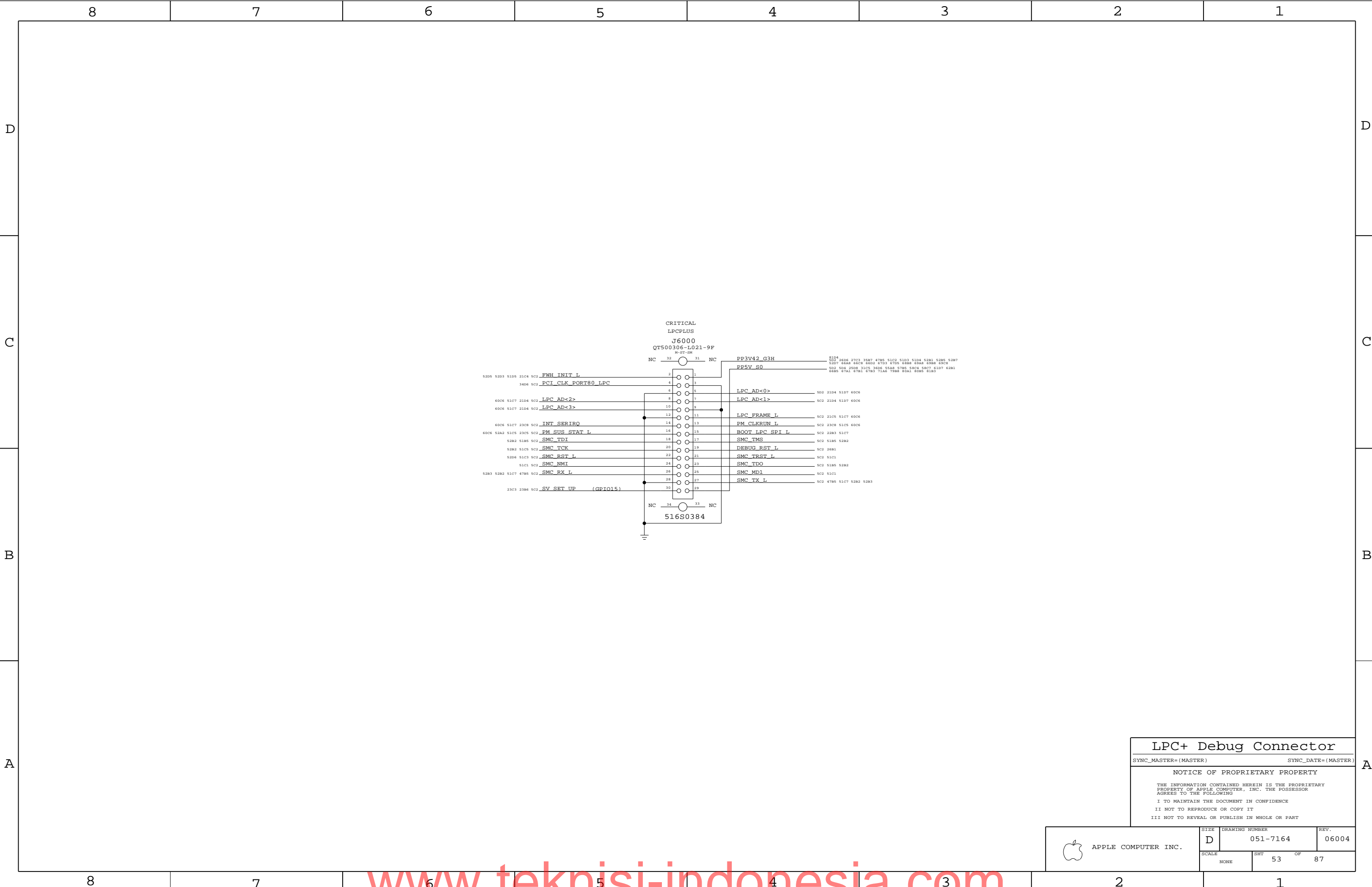


Current & Thermal Sensors			
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D	051-7164	06004	
SCALE		SHT	OF
NONE		49	87









**LPC+ Debug Connector**

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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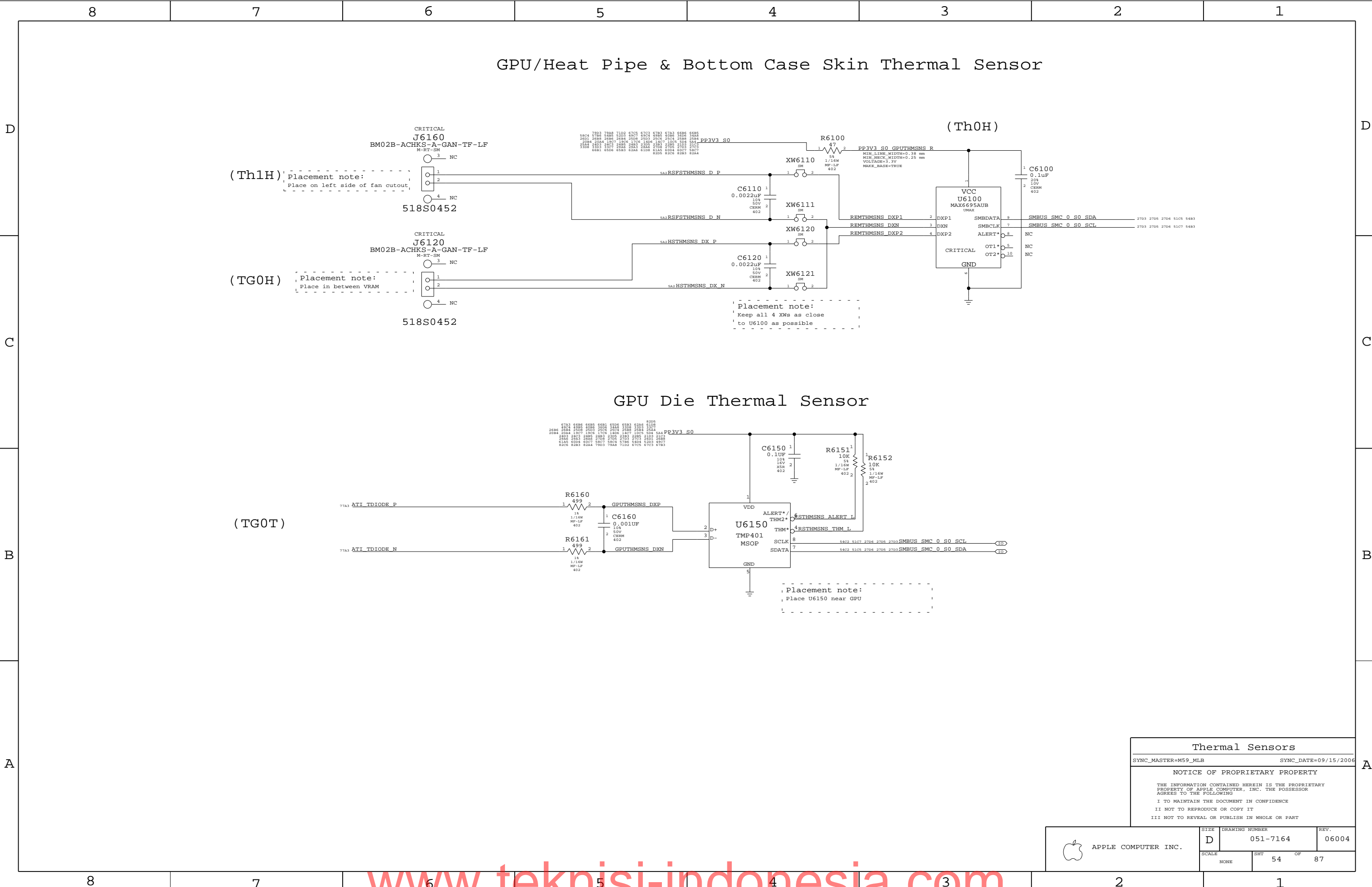
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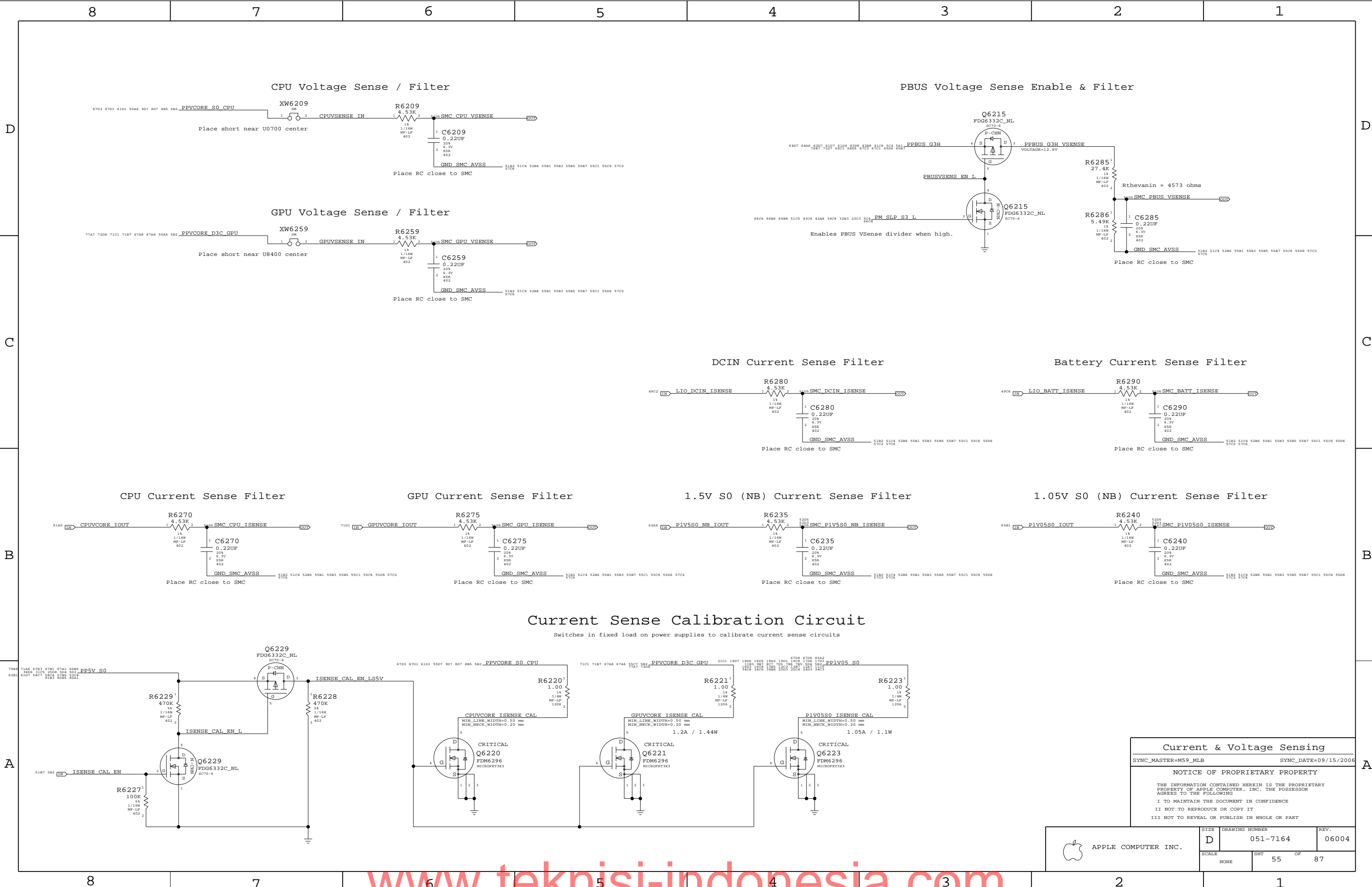
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 53	OF 87

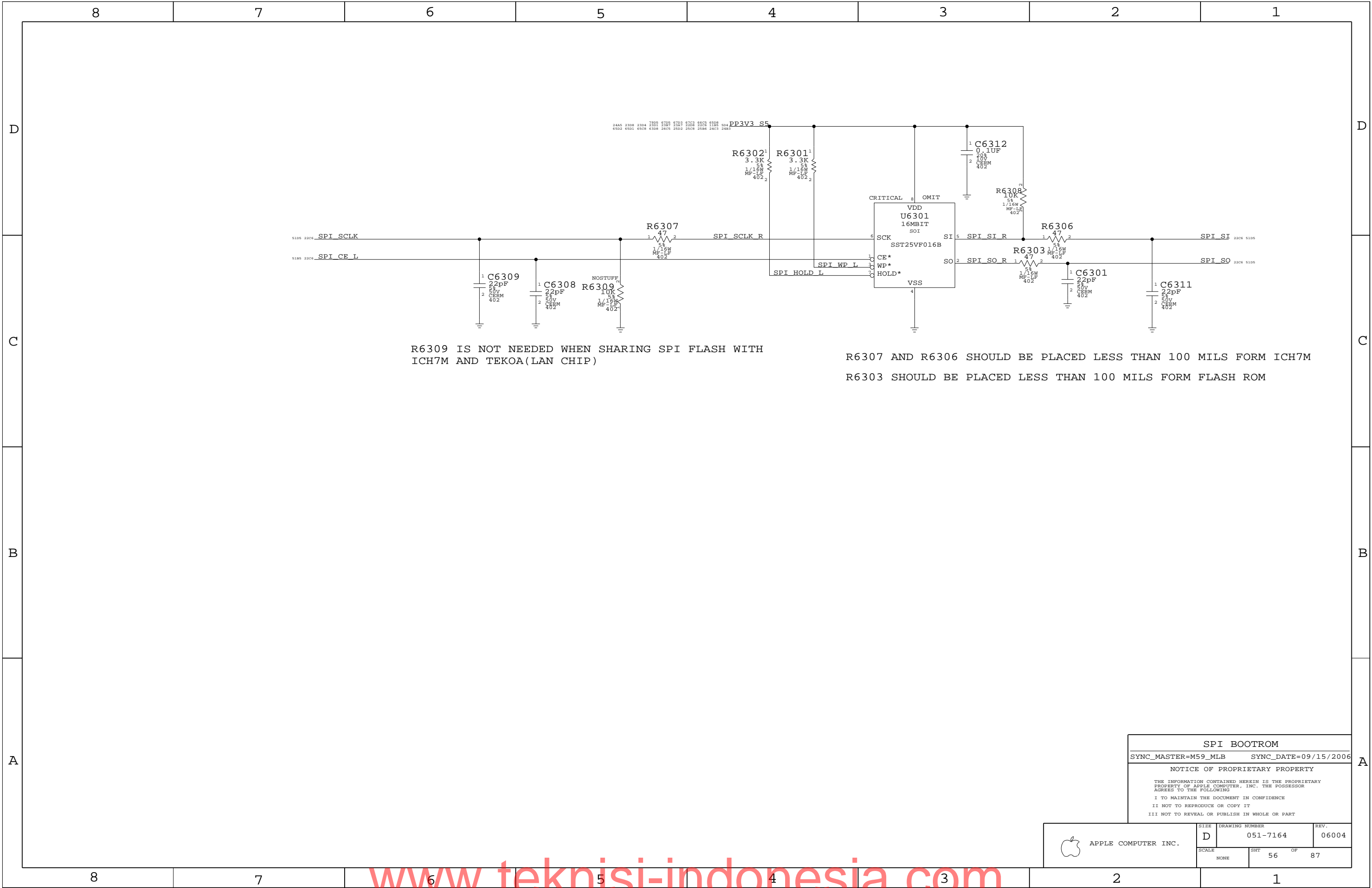


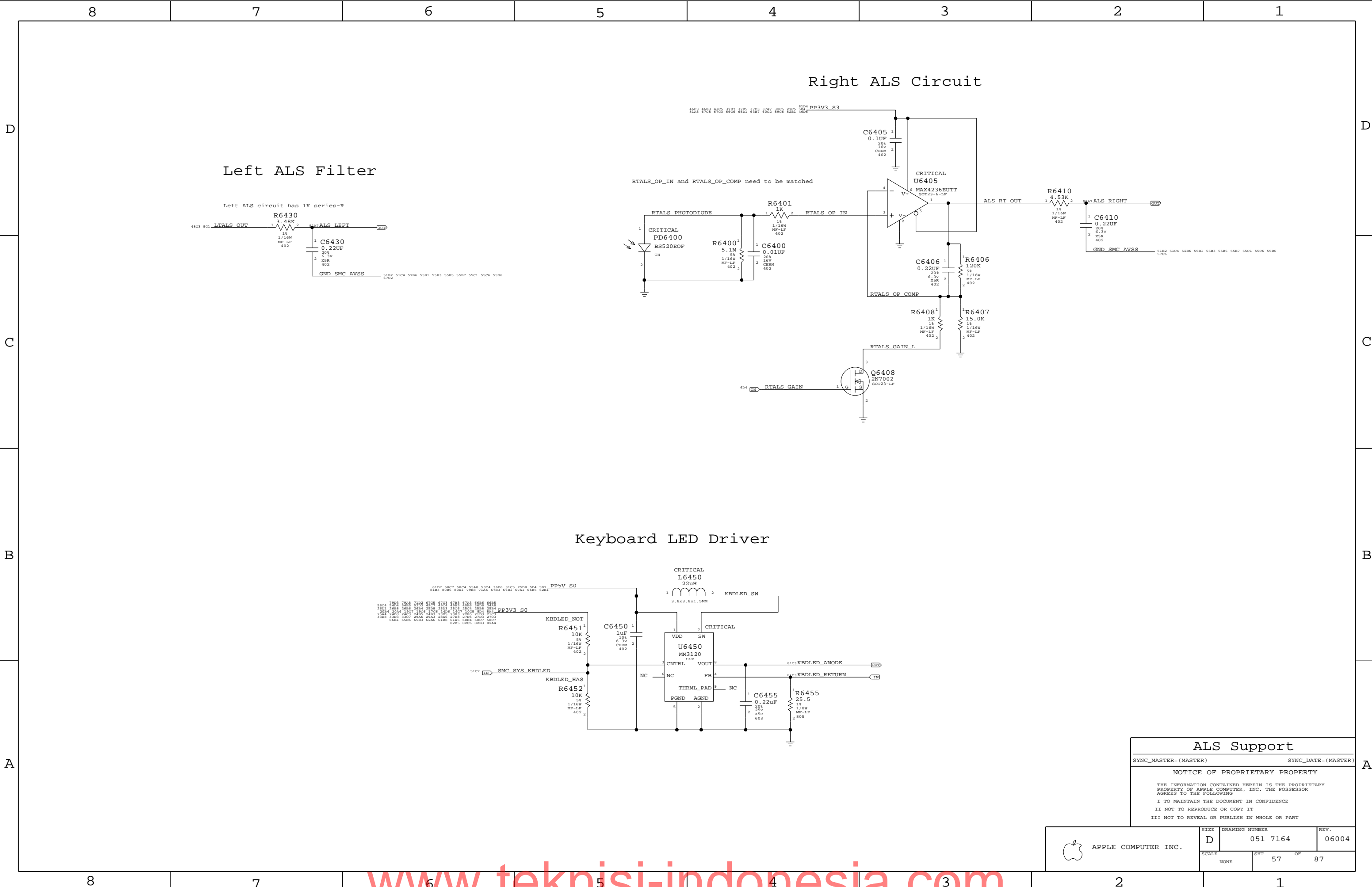




Current & Voltage Sensing		
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	SCALE NONE	SHT 55 OF 87	





ALS Support

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

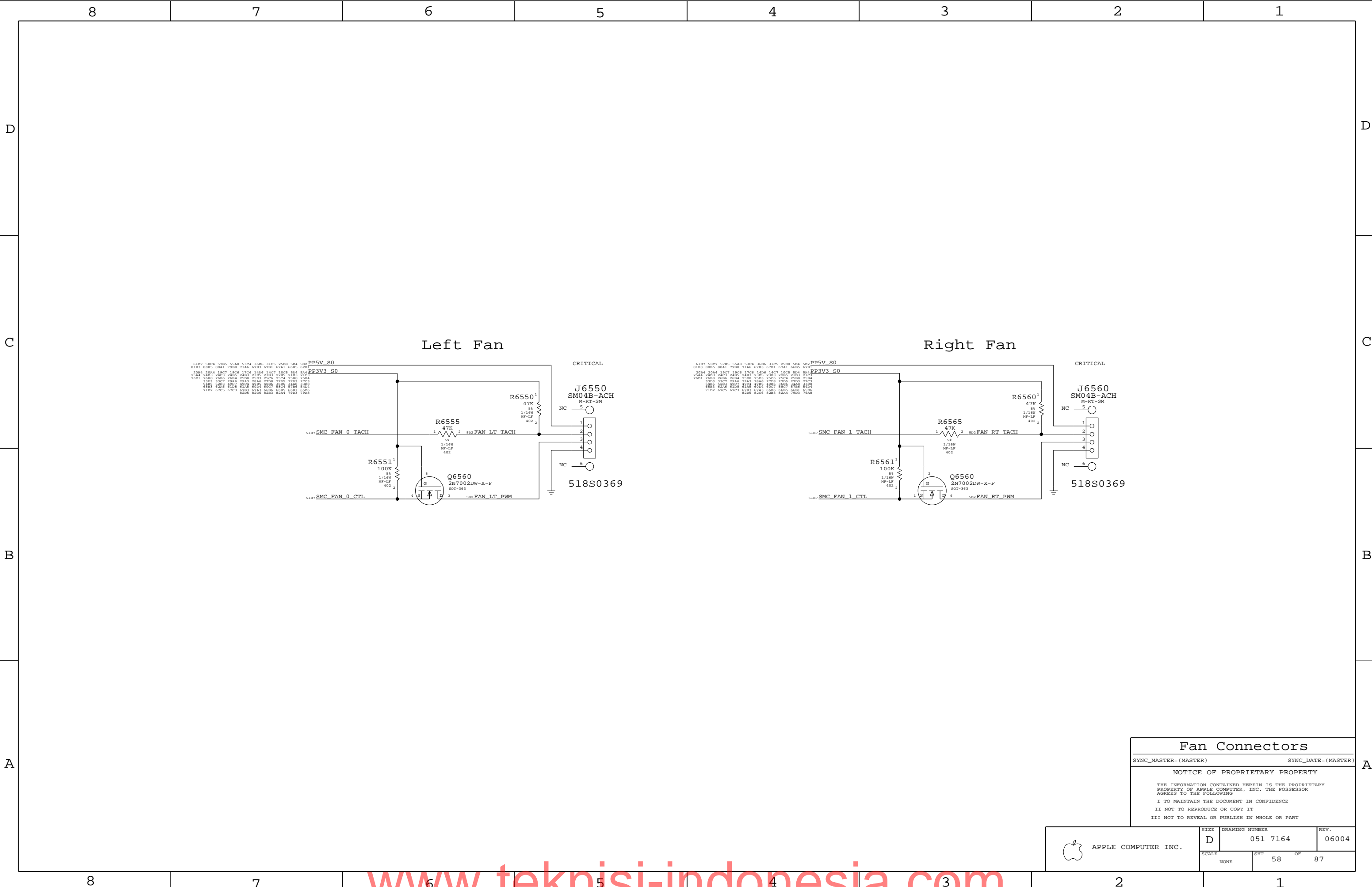
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SCALE		SHT	OF
NONE		57	87



Fan Connectors

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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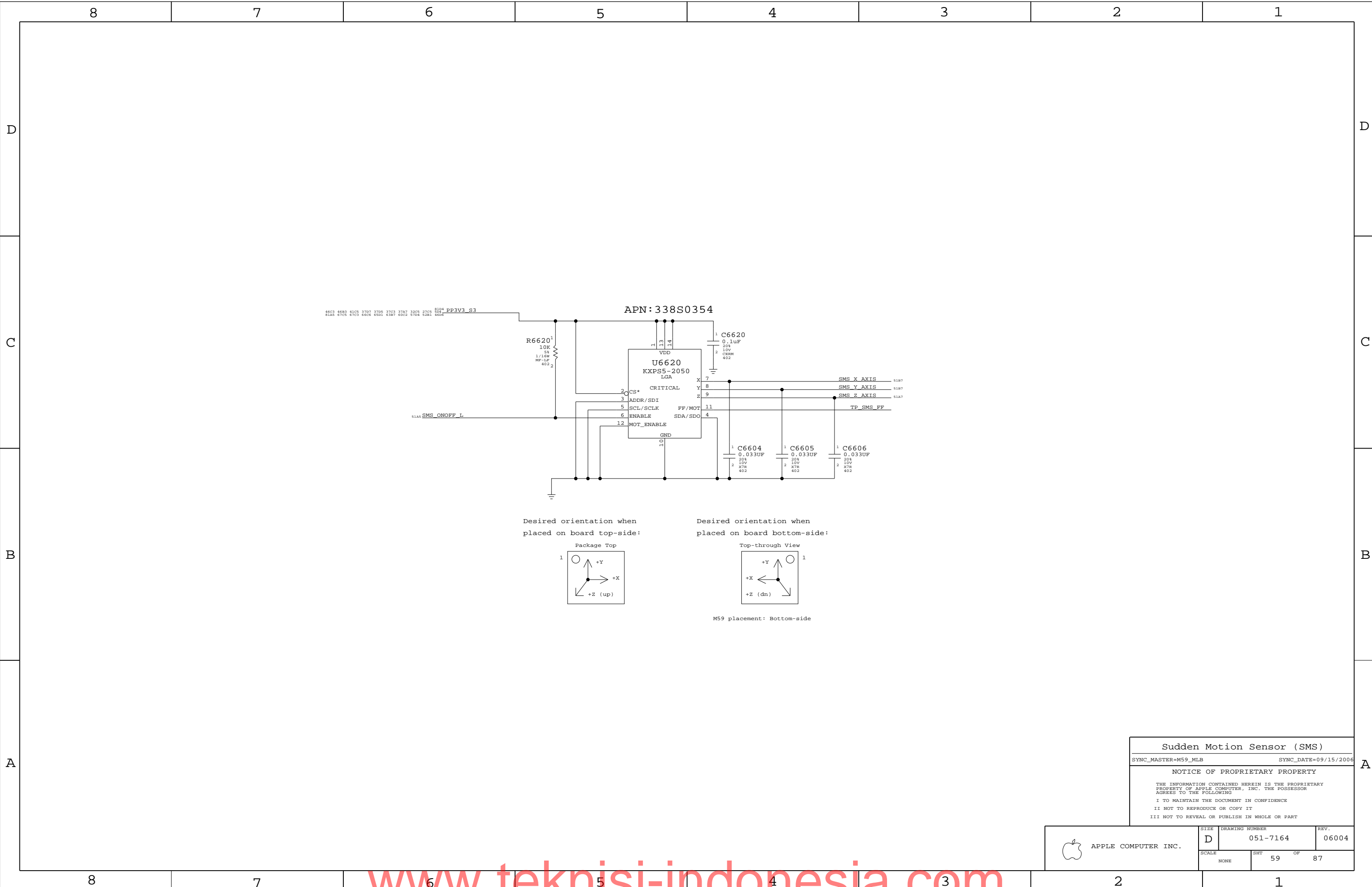
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	SCALE NONE	SHT 58	OF 87



D

C

B

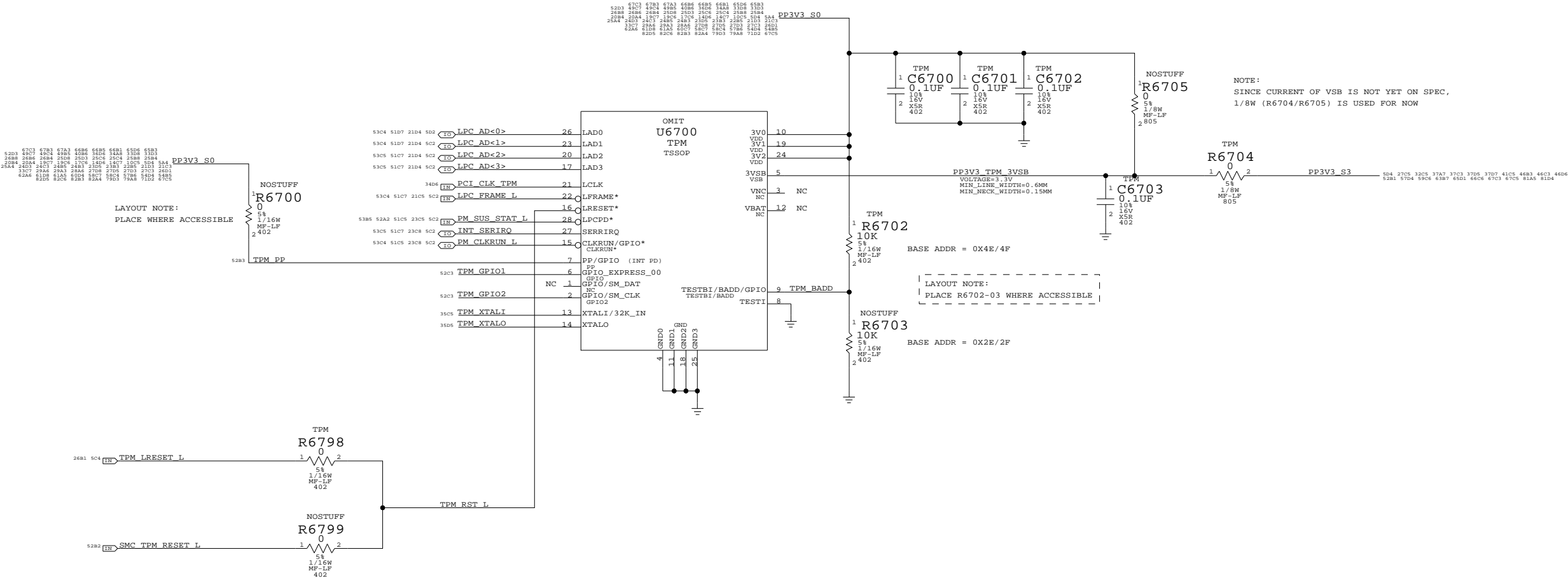
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D

C

B

A



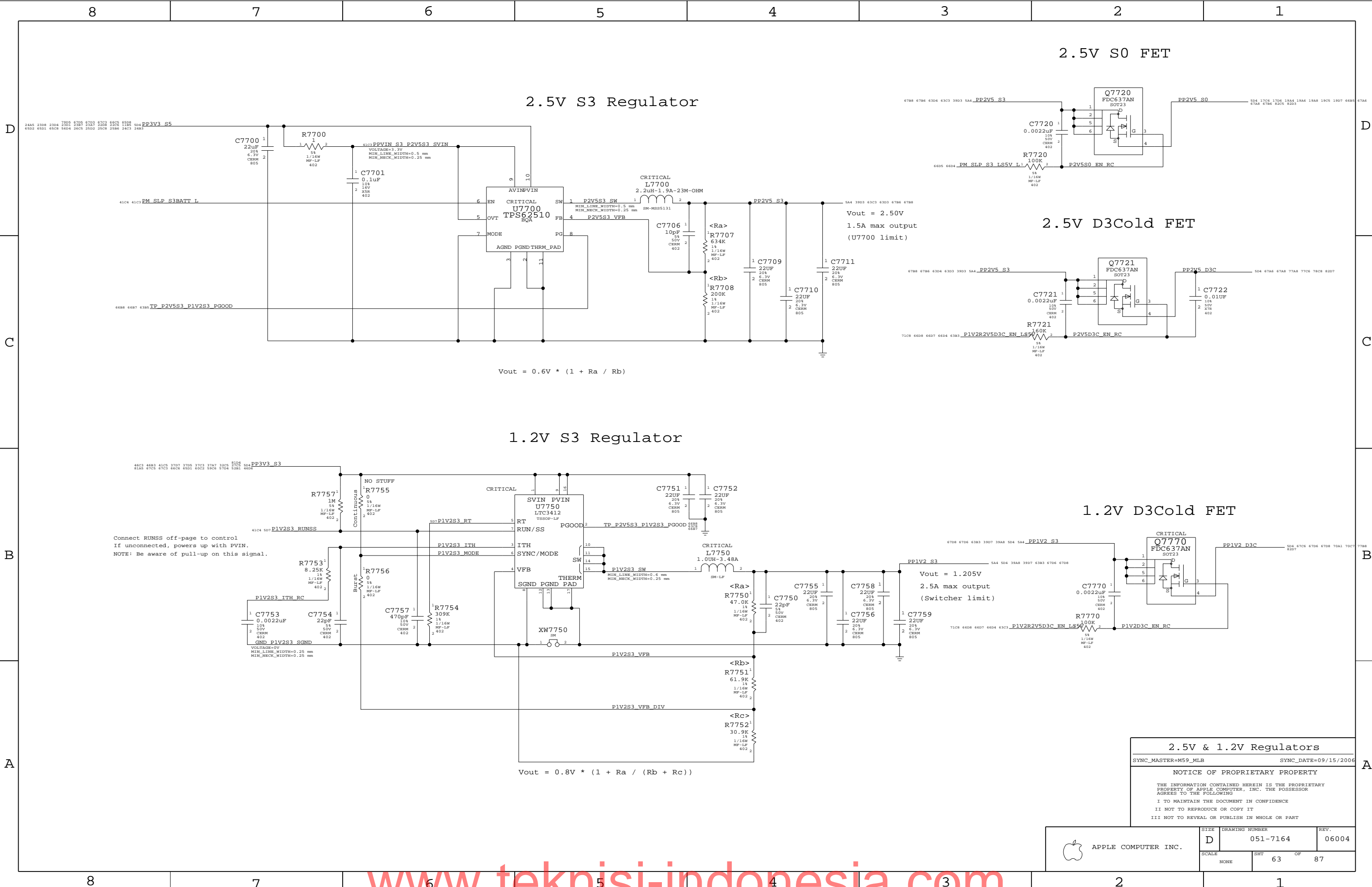
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NOTICE OF PROPRIETARY PROPERTY	
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 60	OF 87









2.5V S3 Regulator


2.5V S0 FET

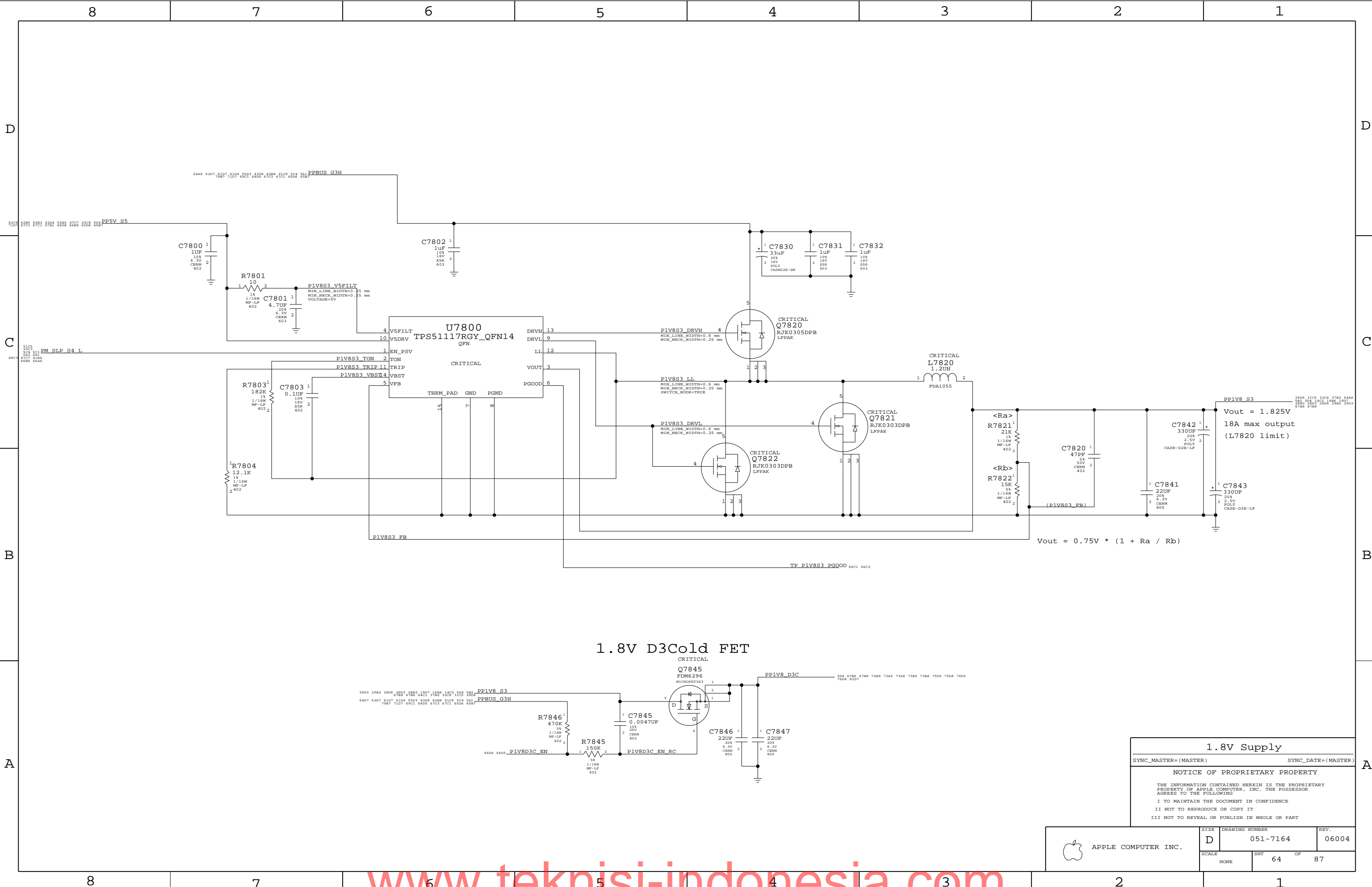
2.5V D3Cold FET

1.2V S3 Regulator

1.2V D3Cold FET

2.5V & 1.2V Regulators		
SYNC_MASTER=M59_MLB		SYNC_DATE=09/15/2006
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	SCALE NONE	SHT 63	OF 87



1.8V D3Cold FET

1.8V Supply

SYNC\_MASTER=(MASTER)

SYNC\_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

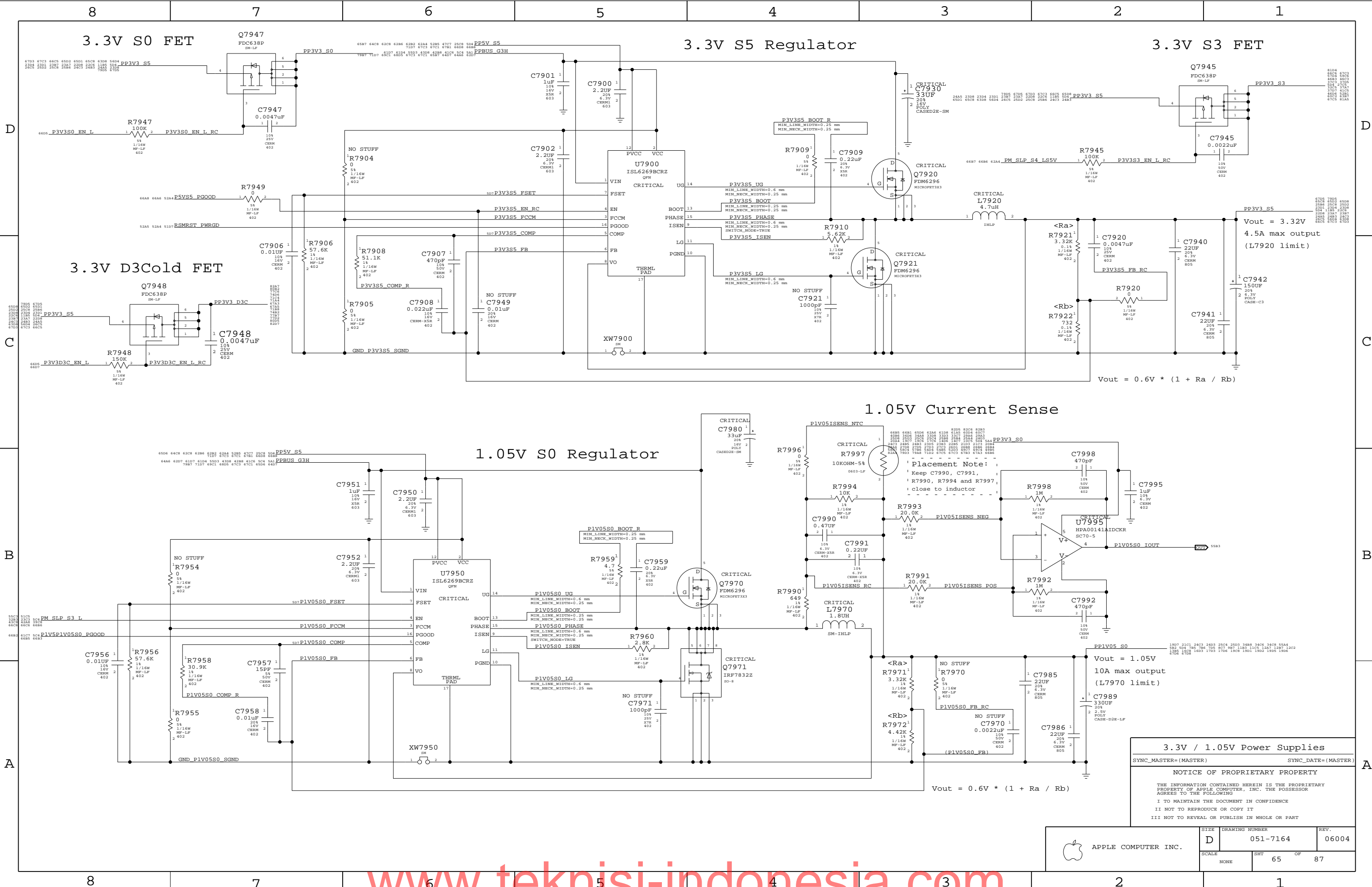
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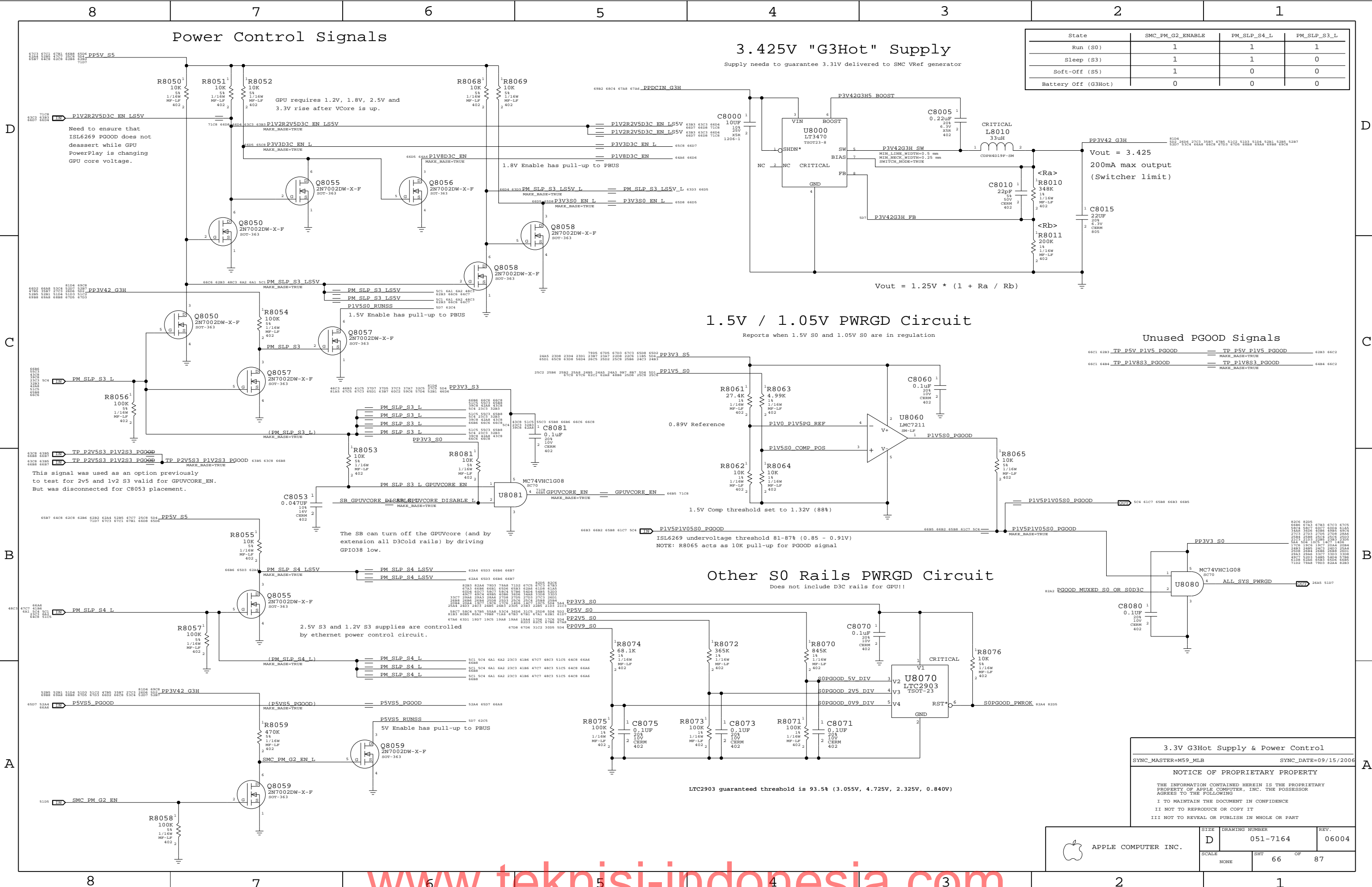
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
SCALE		SHT	OF
NONE		64	87

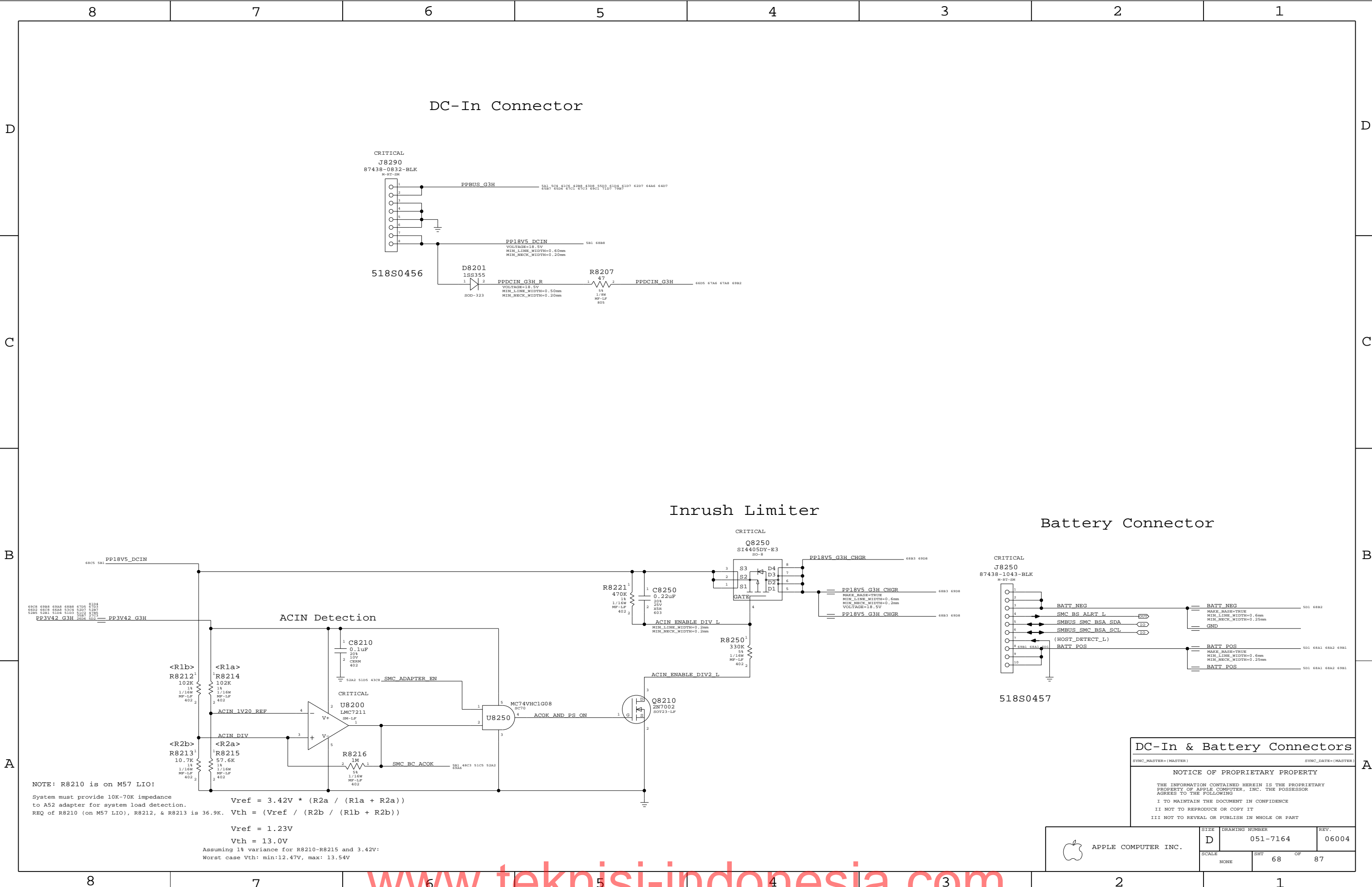




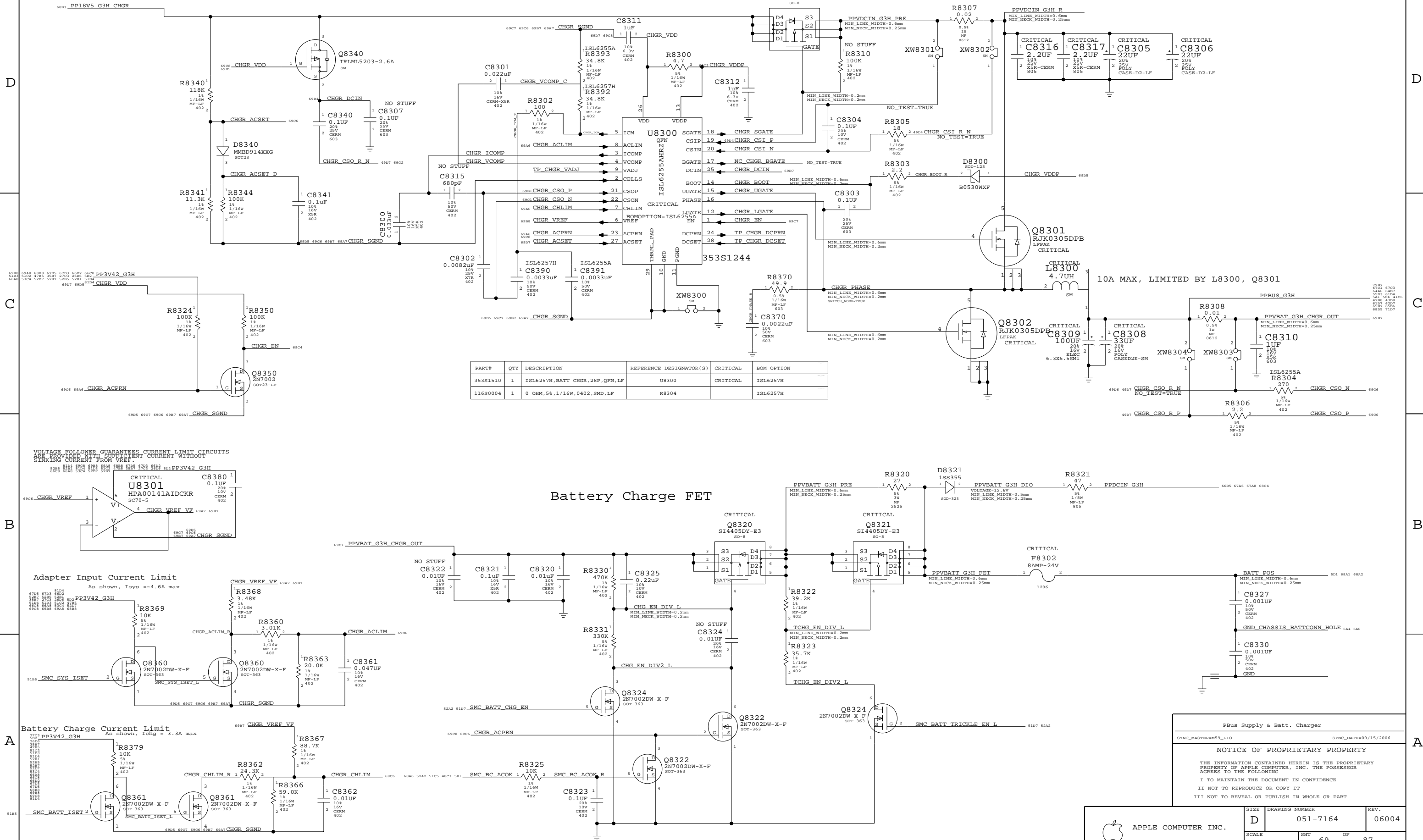








PBus Supply & Battery Charger



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1510	1	ISL6257H, BATT CHGR, 28P, QFN, LF	U8300	CRITICAL	ISL6257H
116S0004	1	0 OHM, 5%, 1/16W, 0402, SMD, LF	R8304		ISL6257H

Battery Charge FET

PBus Supply & Batt. Charger

SYNC\_MASTER=M59\_L10 SYNC\_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

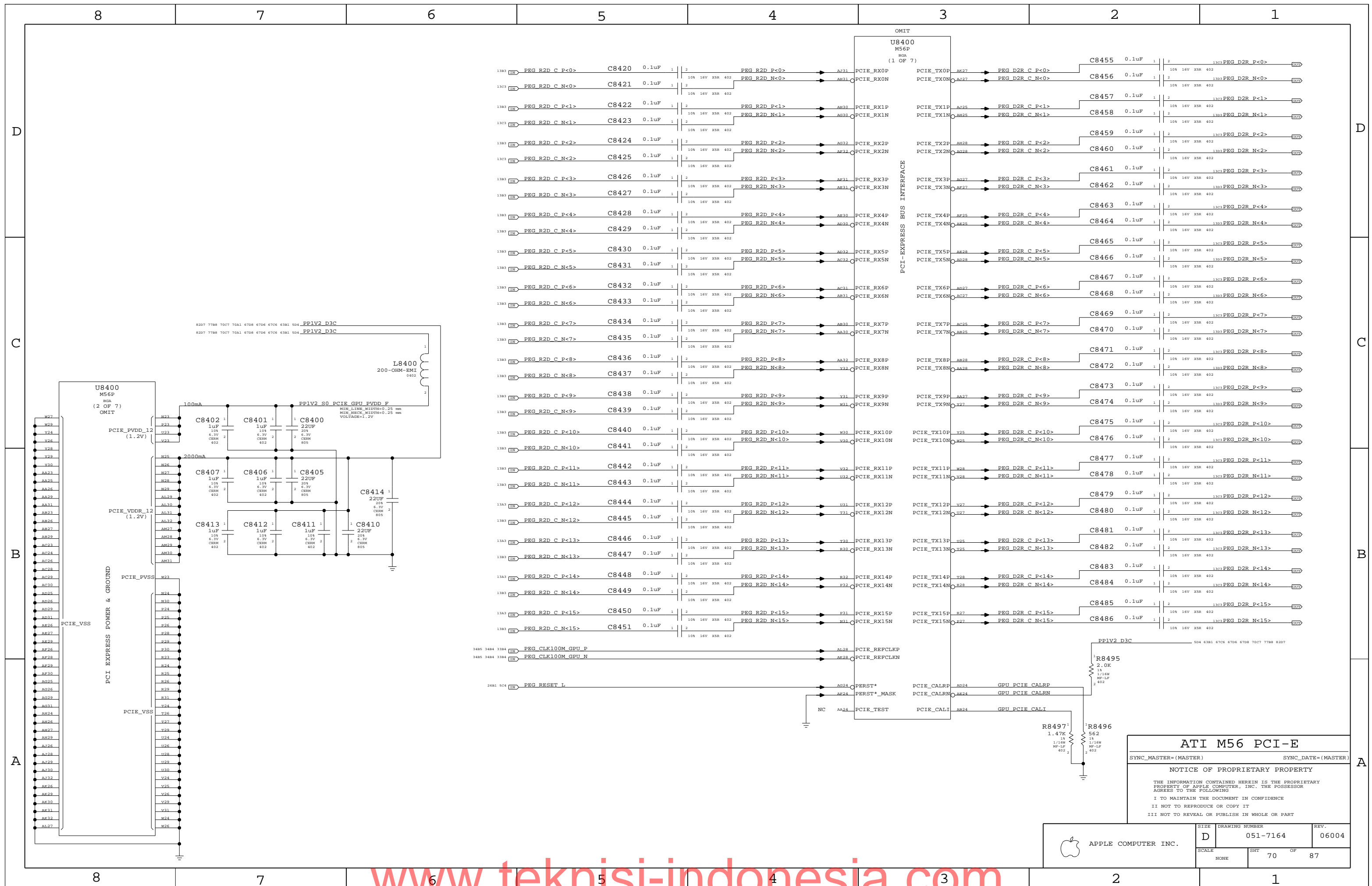
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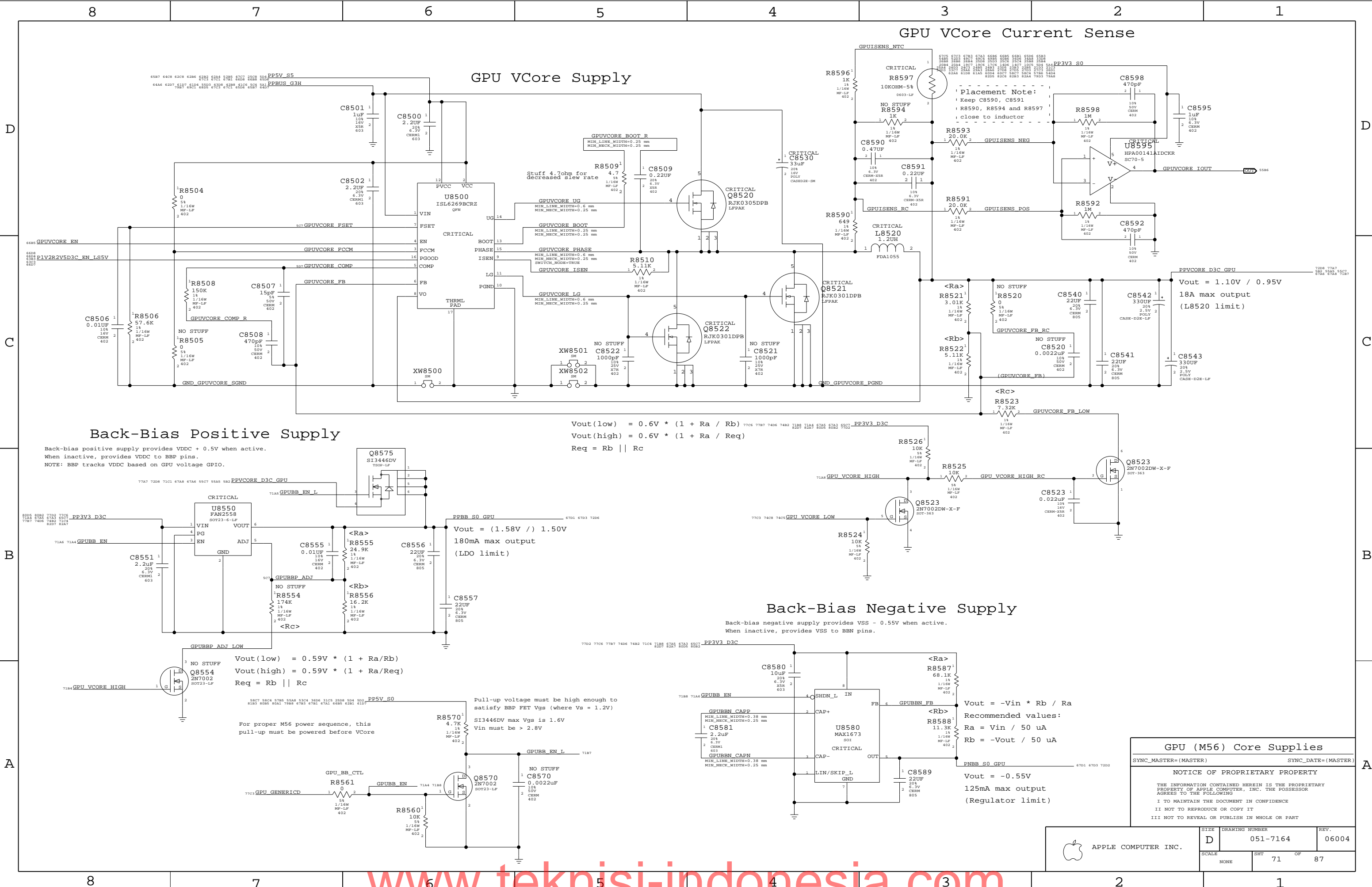
II NOT TO REPRODUCE OR COPY IT

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APPLE COMPUTER INC.	SIZE	D	DRAWING NUMBER	051-7164	REV.	06004
	SCALE	NONE	SHT	69	OF	87







### GPU VCore Supply

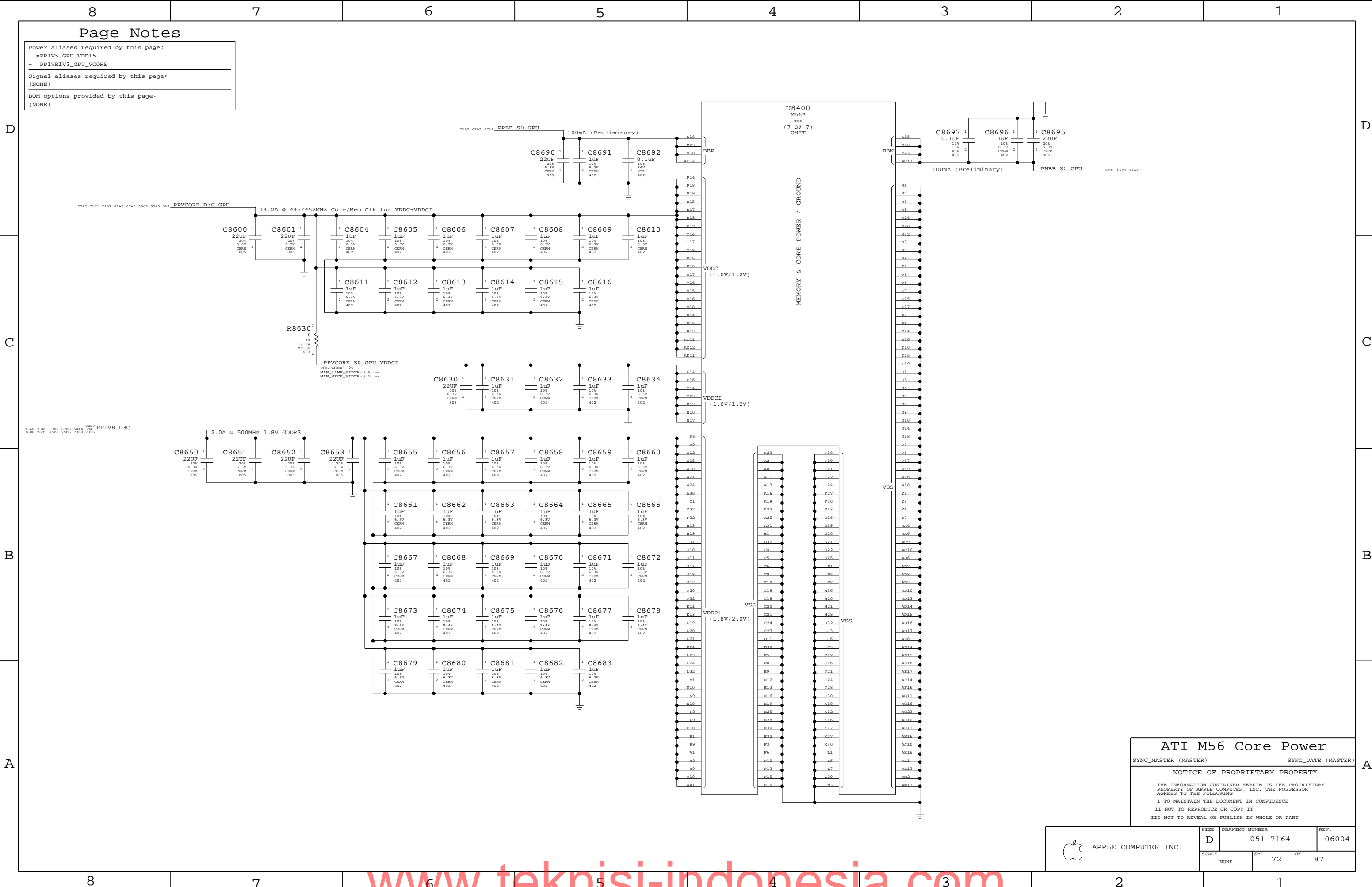
### GPU VCore Current Sense

### Back-Bias Positive Supply

### Back-Bias Negative Supply

GPU (M56) Core Supplies	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
SCALE		SHT	OF
NONE		71	87



Page Notes

Power aliases required by this page:

- =PP1V5\_GPU\_VDD15
- =PP1VR1V3\_GPU\_VCORE

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

ATI M56 Core Power

SYNC\_MASTER=(MASTER)

SYNC\_DATE=(MASTER)

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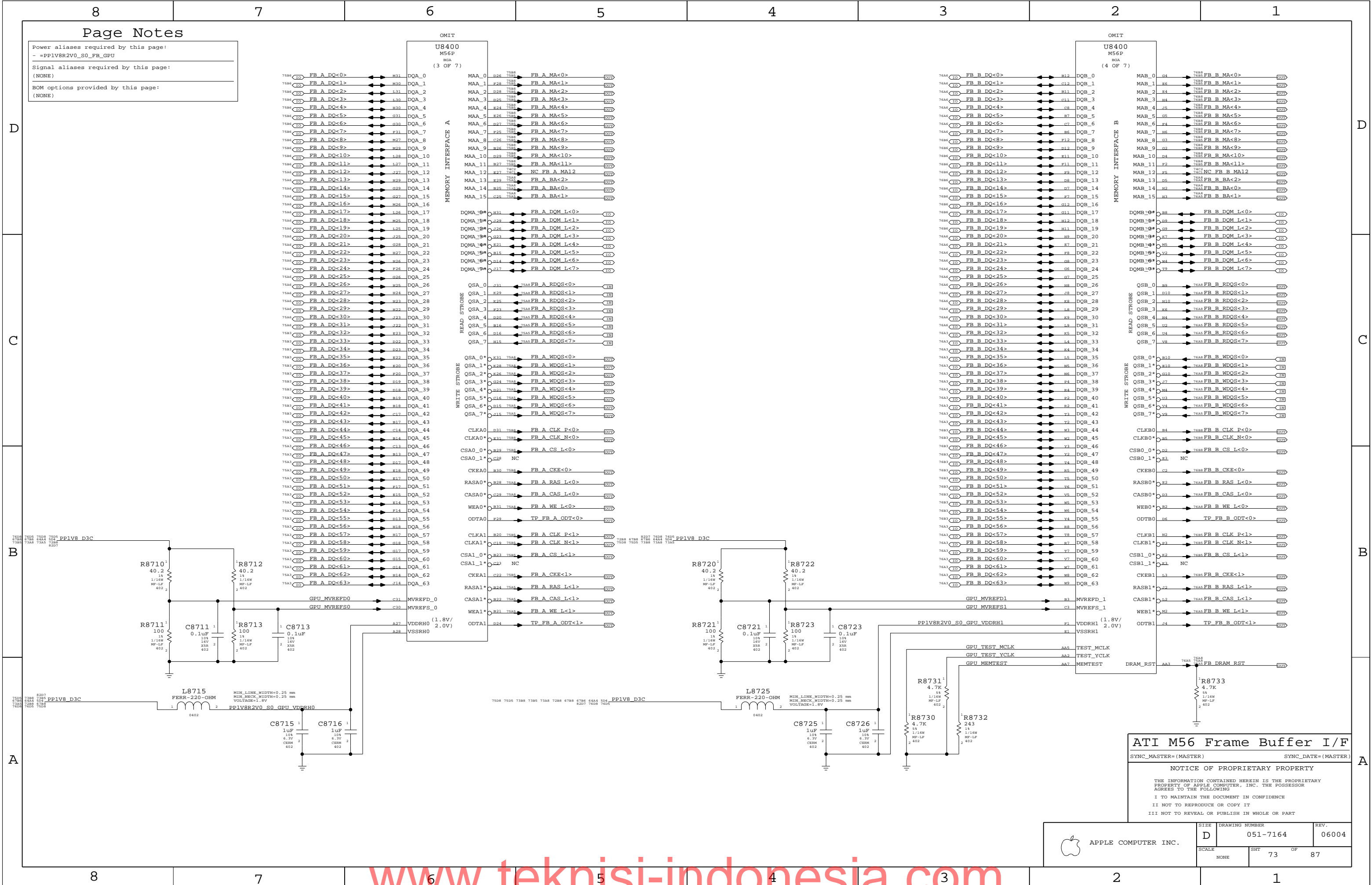
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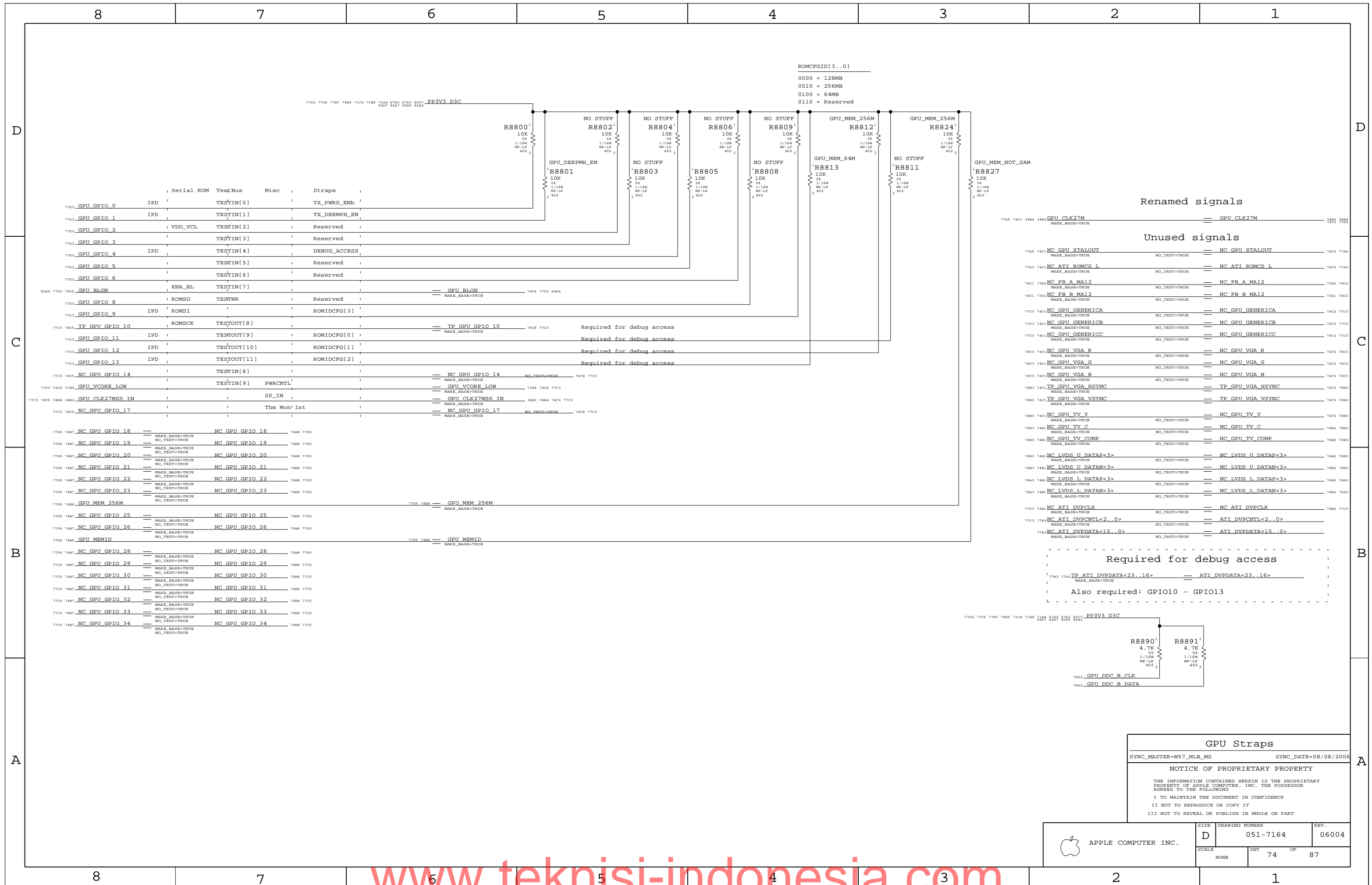
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
SCALE	SHT		
	NONE 72 OF 87		



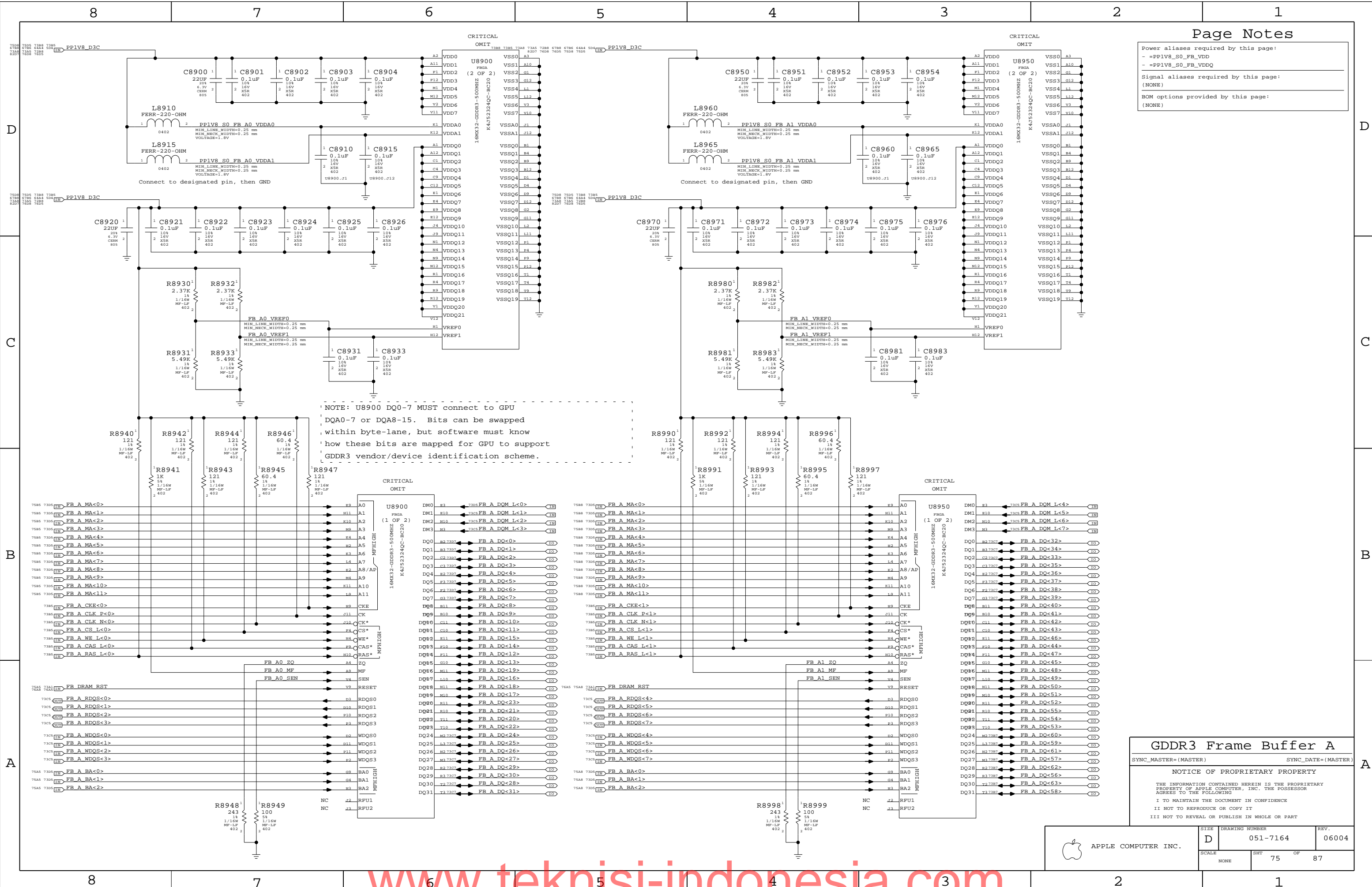




Power aliases required by this page:  
 - =PP1V8\_S0\_FB\_VDD  
 - =PP1V8\_S0\_FB\_VDDQ

Signal aliases required by this page:  
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BOM options provided by this page:  
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## GDDR3 Frame Buffer A

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

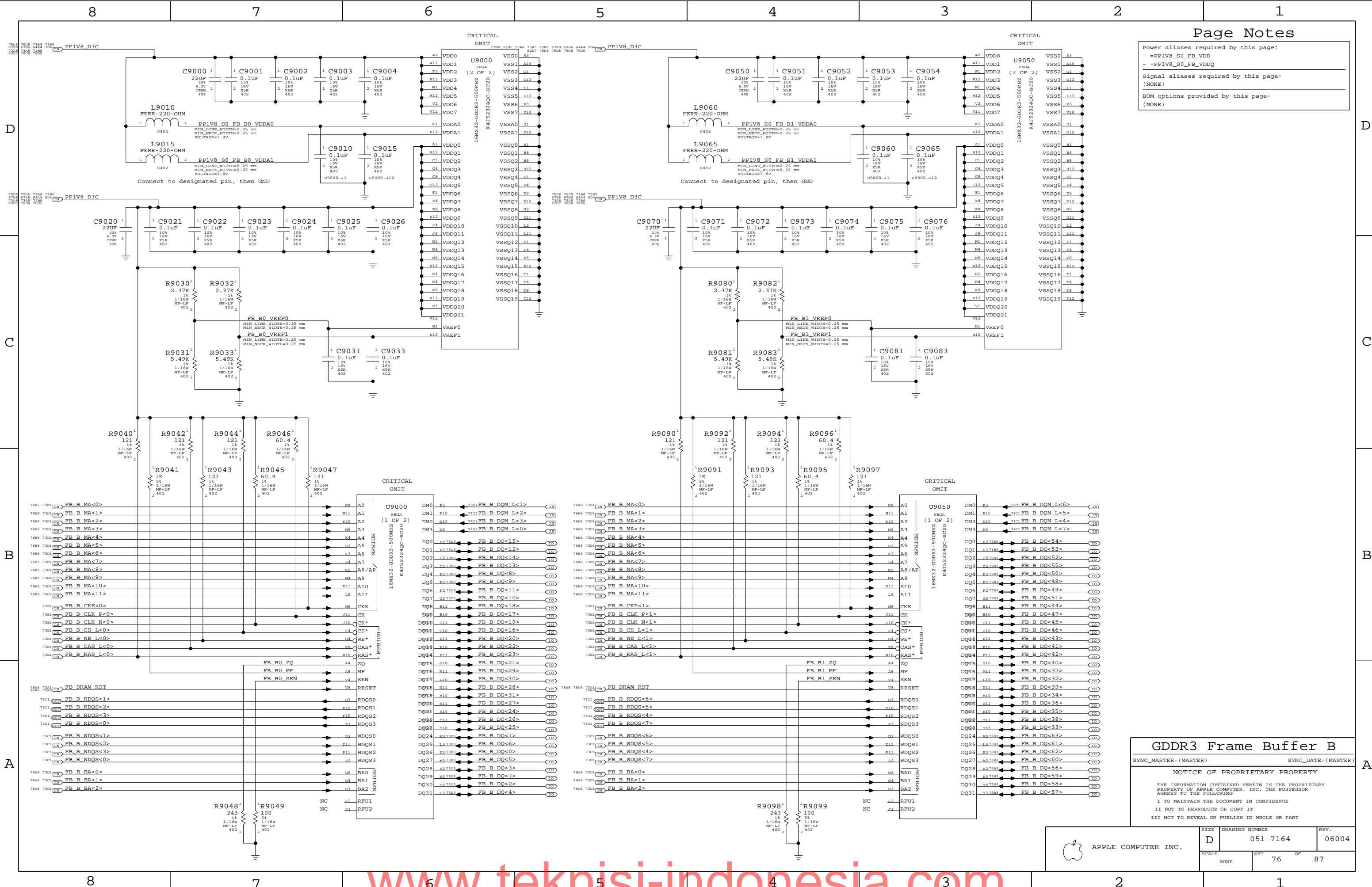
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	75	87



Page Notes

Power aliases required by this page:  
- =PPIV8\_S0\_FB\_VDD  
- =PPIV8\_S0\_FB\_VDDQ

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

GDDR3 Frame Buffer B

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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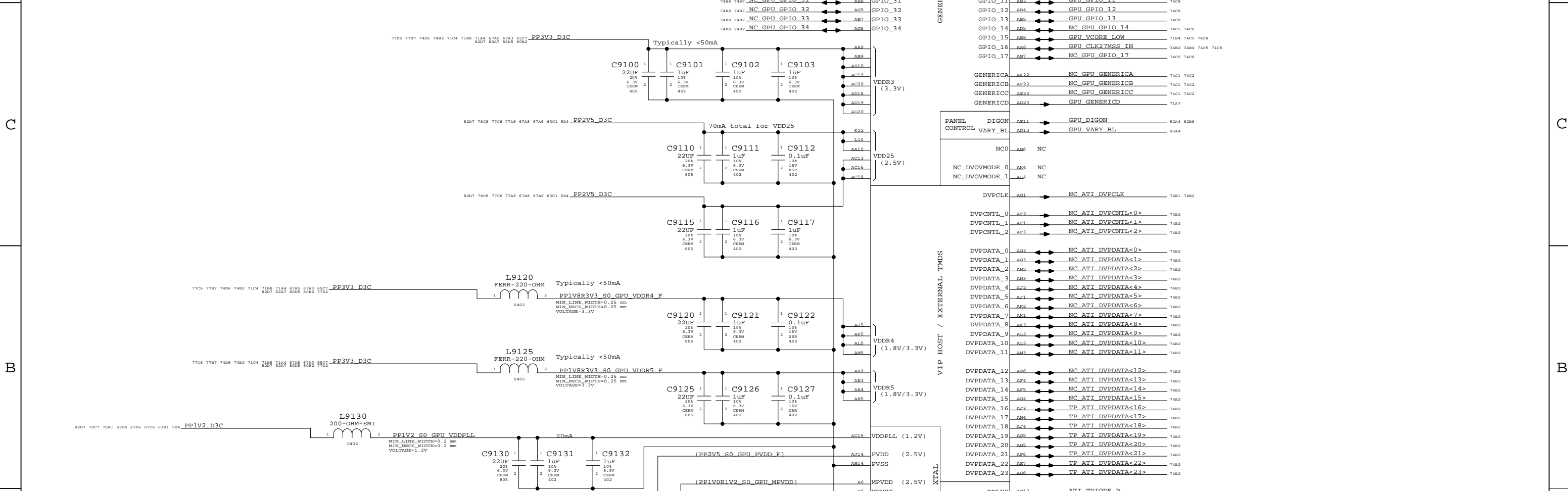
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART


APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
SCALE		SHT	OF
NONE		76	87



8	7	6	5	4	3	2	1
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BOM options provided by this page:  
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
	SCALE	SHT OF	
	NONE	77 OF 87	

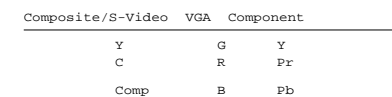
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- =PP2V5_S0_GPU
- =Pp1V8R2V5_S0_GPU_LVDDR
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Signal aliases required by this page:
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SYNC_MASTER= ( MASTER )	SYNC_DATE= ( MASTER )
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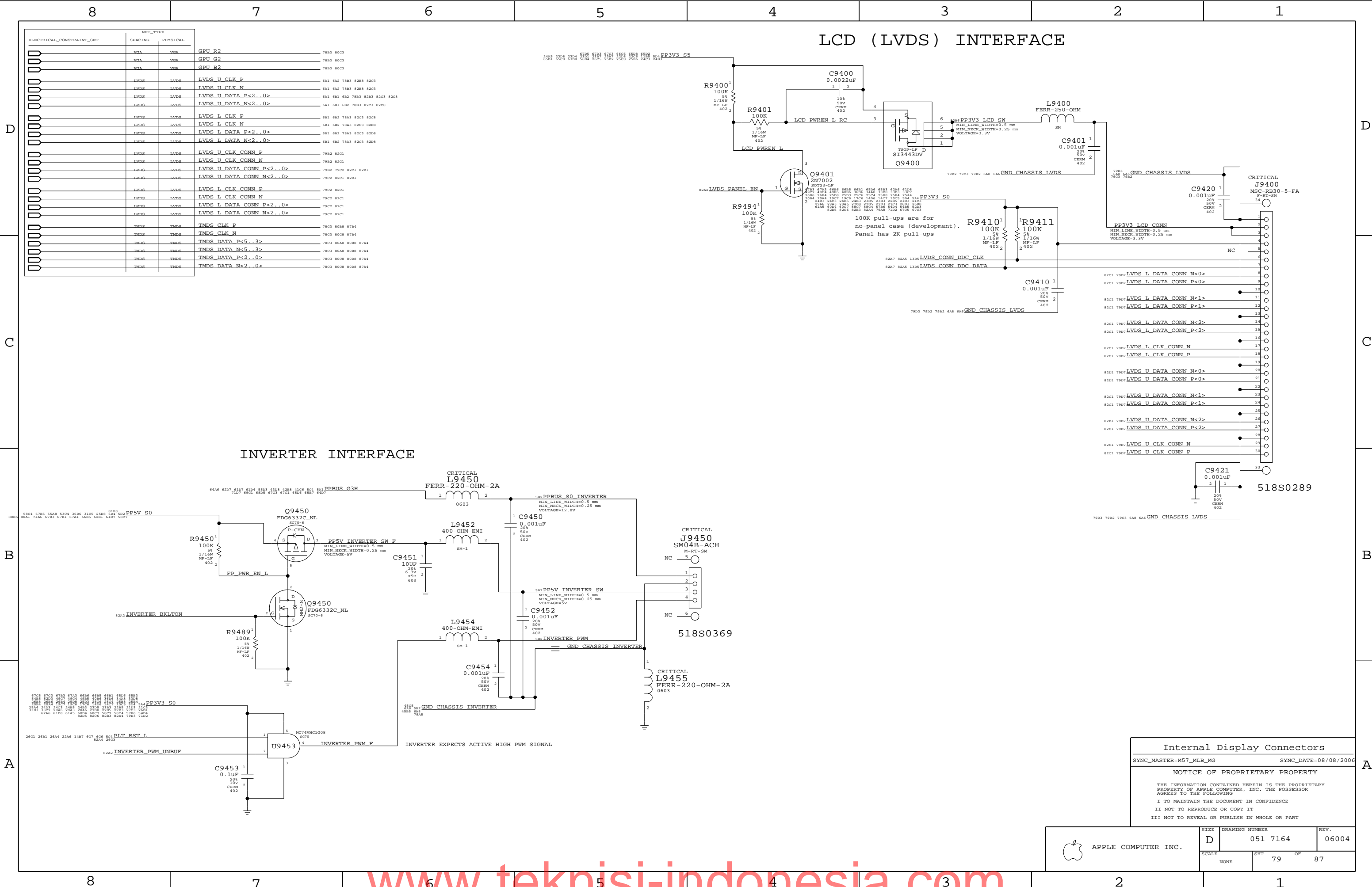
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	D	051-7164	06004
	SCALE	SHT	OF
	NONE	78	87



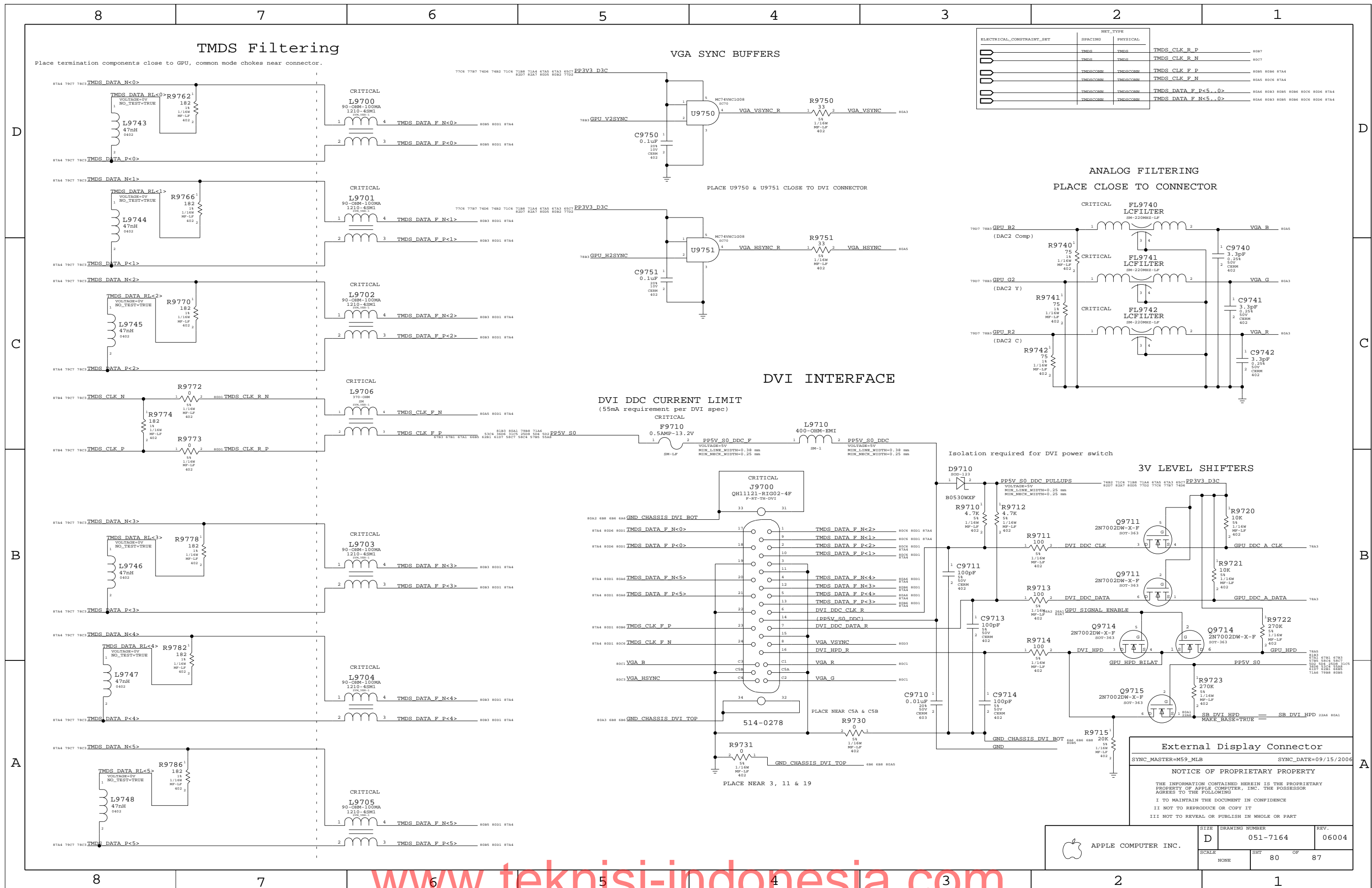
ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	SPACING	PHYSICAL
GPU R2	VGA	VGA
	VGA	VGA
	VGA	VGA
GPU G2	VGA	VGA
	VGA	VGA
	VGA	VGA
GPU B2	VGA	VGA
	VGA	VGA
	VGA	VGA
LVDS U CLK P	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS U CLK N	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS U DATA P<2..0>	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS U DATA N<2..0>	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS L CLK P	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS L CLK N	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS L DATA P<2..0>	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS L DATA N<2..0>	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS U CLK CONN P	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS U CLK CONN N	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS U DATA CONN P<2..0>	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS U DATA CONN N<2..0>	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS L CLK CONN P	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS L CLK CONN N	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS L DATA CONN P<2..0>	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
LVDS L DATA CONN N<2..0>	LVDS	LVDS
	LVDS	LVDS
	LVDS	LVDS
TMDS CLK P	TMDS	TMDS
	TMDS	TMDS
	TMDS	TMDS
TMDS CLK N	TMDS	TMDS
	TMDS	TMDS
	TMDS	TMDS
TMDS DATA P<5..3>	TMDS	TMDS
	TMDS	TMDS
	TMDS	TMDS
TMDS DATA N<5..3>	TMDS	TMDS
	TMDS	TMDS
	TMDS	TMDS
TMDS DATA P<2..0>	TMDS	TMDS
	TMDS	TMDS
	TMDS	TMDS
TMDS DATA N<2..0>	TMDS	TMDS
	TMDS	TMDS
	TMDS	TMDS

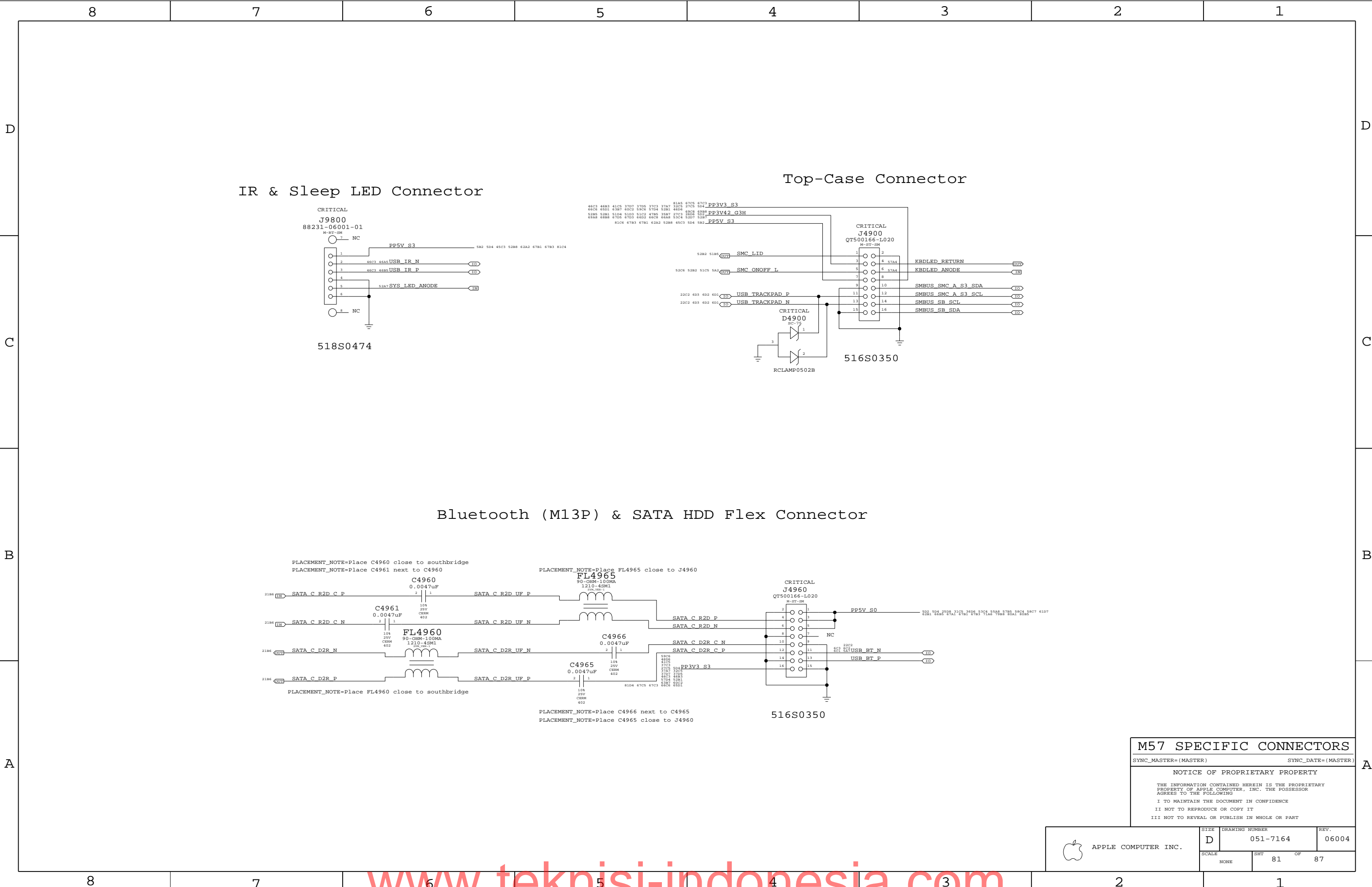
INVERTER INTERFACE

Internal Display Connectors	
SYNC_MASTER=M57_MLB_MG	SYNC_DATE=08/08/2006
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	D	051-7164	06004
SCALE		SHT	79 OF 87
NONE			







IR & Sleep LED Connector

Top-Case Connector

Bluetooth (M13P) & SATA HDD Flex Connector

M57 SPECIFIC CONNECTORS

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	81	87

## LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.

## PGOOD Monitor for GPU Rails

D3CPGOOD\_ALL BOM option stuffs LTC2903 circuit to monitor all D3C rails to qualify D3CPGOOD.  
D3CPGOOD\_3V3 BOM option uses only PP3V3\_D3C to qualify D3CPGOOD.

## LVDS I/F Mux

D

D

C

C

B

B

A

A

## GPU DDC Pass FETs

## LVDS Mux Selection Qualification

Enables the GPU LVDS path in the mux with the qualification that the GPU has turned on panel power and that the panel power has risen to (near) 3.3V. This should eliminate need for LVDS pulldowns

## GPU LVDS I/F

## Panel/Backlight Control Mux

### LVDS Interface Pull-downs

SYNC\_MASTER=M59\_MLB SYNC\_DATE=09/15/2006

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SIZE D DRAWING NUMBER 051-7164 REV. 06004

SCALE NONE SHT 82 OF 87

The drawing area is a large rectangle defined by a grid. The top and bottom edges are labeled with numbers 1 through 8 from right to left. The left and right edges are labeled with letters A through D from bottom to top. The interior of the rectangle is mostly empty, with a small title block in the bottom right corner.

Revision History	
SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
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SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	83	87

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